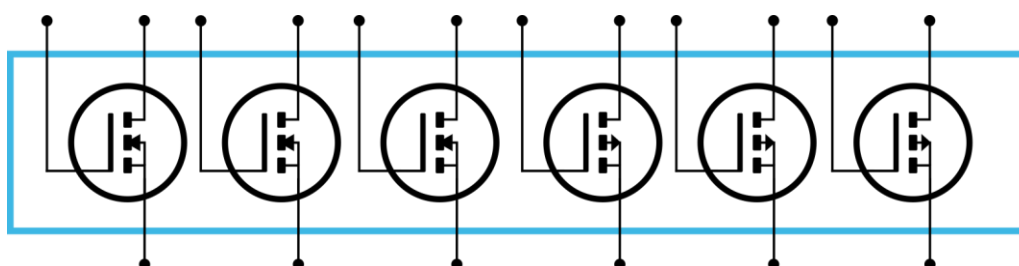
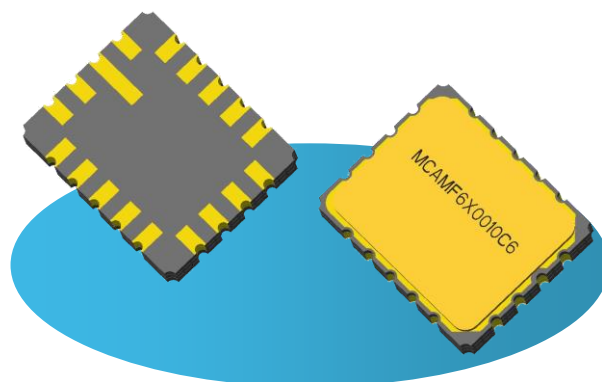


MULTI CHIP ARRAY COMPLEMENTARY 3x 2N7000 3x TP0610 ISOLATED MOSFET TRANSISTORS

MCAMF6X0010C6

- Hermetic MO-042AA (LCC6)
- Low $R_{ds(on)}$
- MOSFET Transistors 3x N-Channel & 3x P-Channel
- High Speed Switching
- High Reliability Screening Options Available



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

		2N7000	TP0610
V_{DS}	Drain - Source Voltage	60V	-60V
V_{GS}	Gate - Source Voltage	$\pm 20\text{V}$	$\pm 20\text{V}$
I_D	Drain Current	200mA	-200mA
I_{DM}	Pulsed Drain Current	500mA	-500mA
$P_D^{(1)}$	Power Dissipation	$T_{sp} = 25^\circ\text{C}$ 1.38W	
		Derate Above 25°C 11.11mW/ $^\circ\text{C}$	
	Total Power Dissipation ⁽²⁾	$T_{sp} = 25^\circ\text{C}$ 4.16W	
		Derate Above 25°C 33.33mW/ $^\circ\text{C}$	
T_J	Junction Temperature Range	-55 to +150 $^\circ\text{C}$	
T_{stg}	Storage Temperature Range	-55 to +150 $^\circ\text{C}$	

THERMAL PROPERTIES

Symbols	Parameters	Max.	Units
$R_{\theta JSP}^{(1)(3)}$	Thermal Resistance, Junction To Solder Pad (Per Device)	90	$^\circ\text{C}/\text{W}$
$R_{\theta JSP}^{(2)(3)}$	Thermal Resistance, Junction To Solder Pad (Package)	30	$^\circ\text{C}/\text{W}$

Notes

- (1) One device conducting only.
- (2) With all parts conducting, maximum power dissipation per device = 694mW, limited by maximum junction temperature.
- (3) Stated $R_{\theta JSP}$ properties assume infinite heatsink.

Semelab Limited reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

Semelab Limited

Coventry Road, Lutterworth, Leicestershire, LE17 4JB

Telephone: +44 (0) 1455 556565
Fax: +44 (0) 1455 552612

Email: sales@semelab-tt.com

Website: <http://www.semelab-tt.com>

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2N7000 ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ.	Max.	Units
$V_{(BR)DSS}^{(4)}$	Drain - Source Breakdown Voltage	$I_D = 10\mu\text{A}$ $V_{GS} = 0\text{V}$	60	70		V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 0.25\text{mA}$	0.8		3.0	
I_{GSS}	Gate - Body Leakage Current	$V_{GS} = \pm 20\text{V}$ $V_{DS} = 0\text{V}$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$ $V_{GS} = 0\text{V}$			1.0	μA
		$T_A = 125^\circ\text{C}$			1.0	mA
$I_{D(on)}^{(4)}$	On - State Drain Current	$V_{DS} \geq 2 V_{DS(on)}$ $V_{GS} = 4.5\text{V}$	75			mA
$R_{DS(on)}^{(4)}$	Drain - Source On Resistance	$V_{GS} = 10\text{V}$ $I_D = 0.5\text{A}$			5	Ω
		$T_A = 125^\circ\text{C}$			9	
$V_{DS(on)}^{(4)}$	Drain - Source On Voltage	$V_{GS} = 4.5\text{V}$ $I_D = 75\text{mA}$			0.4	V
		$V_{GS} = 10\text{V}$ $I_D = 0.5\text{A}$			2.5	
$g_{fs}^{(4)}$	Forward Transconductance	$V_{GS} = 10\text{V}$ $I_D = 0.5\text{A}$	100			mS

2N7000 DYNAMIC CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ.	Max.	Units
$C_{iss}^{(5)}$	Input Capacitance	$V_{DS} = 25\text{V}$ $V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$			60	pF
$C_{oss}^{(5)}$	Output Capacitance				25	
$C_{rss}^{(5)}$	Reverse Transfer Capacitance				5	
$t_{on}^{(5)}$	Turn - On Time	$V_{DD} = 30\text{V}$ $V_{GEN} = 10\text{V}$ $R_L = 150\Omega$			10	ns
$t_{off}^{(5)}$	Turn - Off Time		$R_G = 25\Omega$ $I_D = 0.2\text{A}$			

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TP0610 ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ.	Max.	Units
$V_{(BR)DSS}^{(4)}$	Drain - Source Breakdown Voltage	$I_D = -10\mu\text{A}$ $V_{GS} = 0\text{V}$	-60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = -0.25\text{mA}$	-1.0		-3.5	
I_{GSS}	Gate - Body Leakage Current	$V_{GS} = \pm 20\text{V}$ $V_{DS} = 0\text{V}$			± 10	μA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -48\text{V}$ $V_{GS} = 0\text{V}$			-10	μA
		$T_A = 125^\circ\text{C}$			-1.0	mA
$I_{D(on)}^{(4)}$	On - State Drain Current	$V_{DS} = -4.5\text{V}$ $V_{GS} = -10\text{V}$	-50			mA
$R_{DS(on)}^{(4)}$	Drain - Source On Resistance	$V_{GS} = -10\text{V}$ $I_D = -0.2\text{A}$			10	Ω
		$T_A = 125^\circ\text{C}$		12	18	
V_{SD}	Diode Forward Voltage	$I_{SD} = -200\text{mA}$ $V_{GS} = 0\text{V}$			-1.4	V
$g_{fs}^{(4)}$	Forward Transconductance	$V_{GS} = -10\text{V}$ $I_D = -100\text{mA}$	80			mS

TP0610 DYNAMIC CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ.	Max.	Units
$C_{iss}^{(5)}$	Input Capacitance	$V_{DS} = -25\text{V}$ $V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$		45	60	pF
$C_{oss}^{(5)}$	Output Capacitance			22	30	
$C_{rss}^{(5)}$	Reverse Transfer Capacitance			5	8	
$t_{on}^{(5)}$	Turn - On Time	$V_{DD} = -25\text{V}$ $I_D = -500\text{mA}$ $R_G = 25\Omega$		9	13	ns
$t_{off}^{(5)}$	Turn - Off Time			9	13	

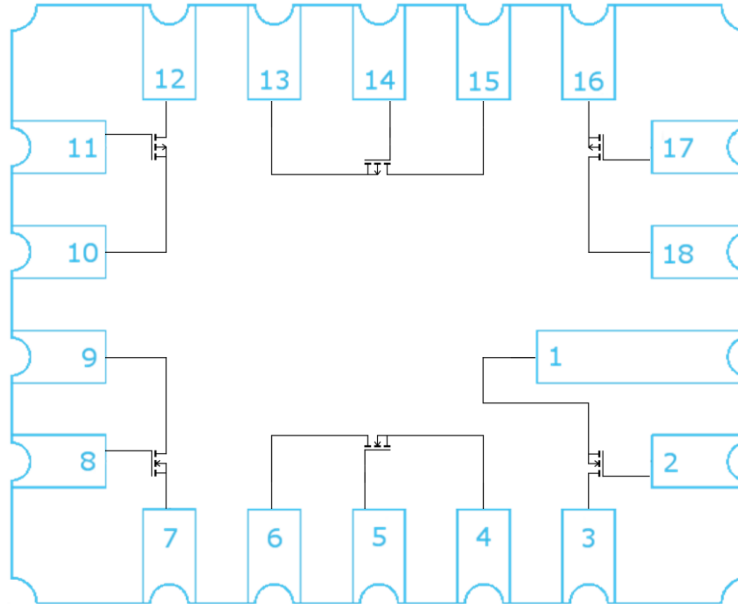
Notes

- (4) Pulse Width $\leq 380\mu\text{s}$, duty cycle $\delta \leq 2\%$.
(5) Characteristics by design.

MULTI CHIP ARRAY 3x 2N7000 3x TP0610
ISOLATED MOSFET TRANSISTORS

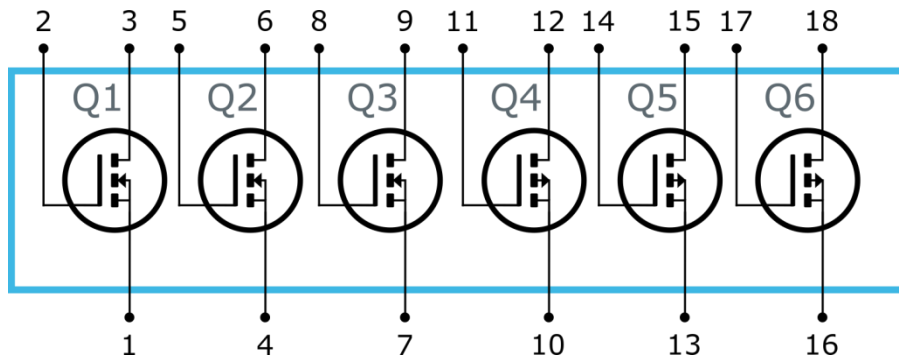
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INTERNAL LAYOUT VISUALISATION



(Underside View)

PACKAGE PIN CONNECTIONS



N-CHANNEL DEVICES : Q1 - Q3

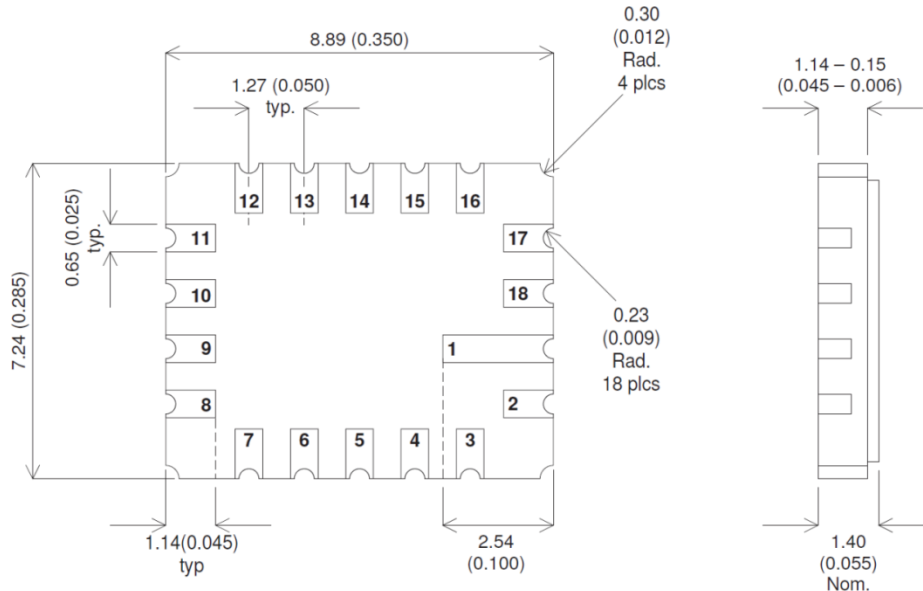
P-CHANNEL DEVICES : Q4 - Q6

Pin	Device	Connection	Pin	Device	Connection
1	Q1	Source	10	Q4	Source
2	Q1	Gate	11	Q4	Gate
3	Q1	Drain	12	Q4	Drain
4	Q2	Source	13	Q5	Source
5	Q2	Gate	14	Q5	Gate
6	Q2	Drain	15	Q5	Drain
7	Q3	Source	16	Q6	Source
8	Q3	Gate	17	Q6	Gate
9	Q3	Drain	18	Q6	Drain

MULTI CHIP ARRAY 3x 2N7000 3x TP0610 ISOLATED MOSFET TRANSISTORS MCAMF6X0010C6

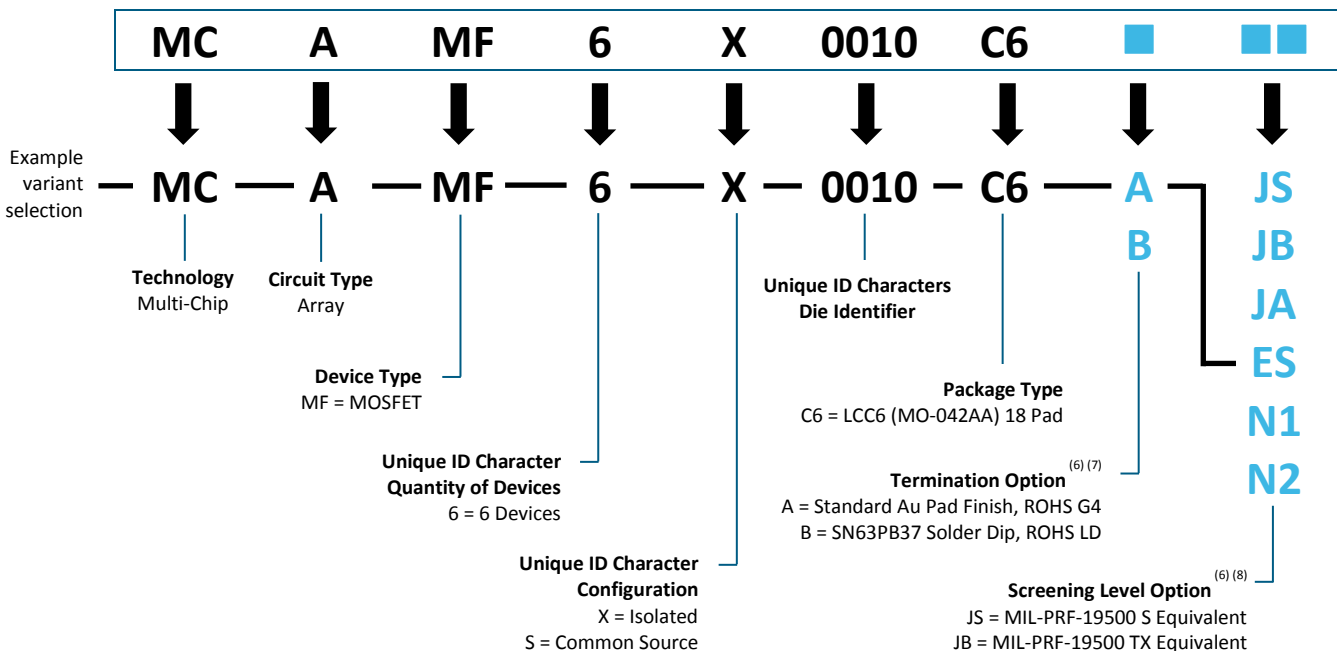
MECHANICAL DATA

Dimensions in mm (inches)



**C6 (MO-042AA)
(Underside View)**

PART VARIANT OPTIONS ⁽⁶⁾



Notes

- (6) Part variant options (termination, screening level) to be specified at point of order.
- (7) LD = e0, G4 = e4, as defined in J-STD-609 2nd Level Interconnect Category.
- (8) Please enquire with customer services regarding other requirements (pin connections, termination & screening level).