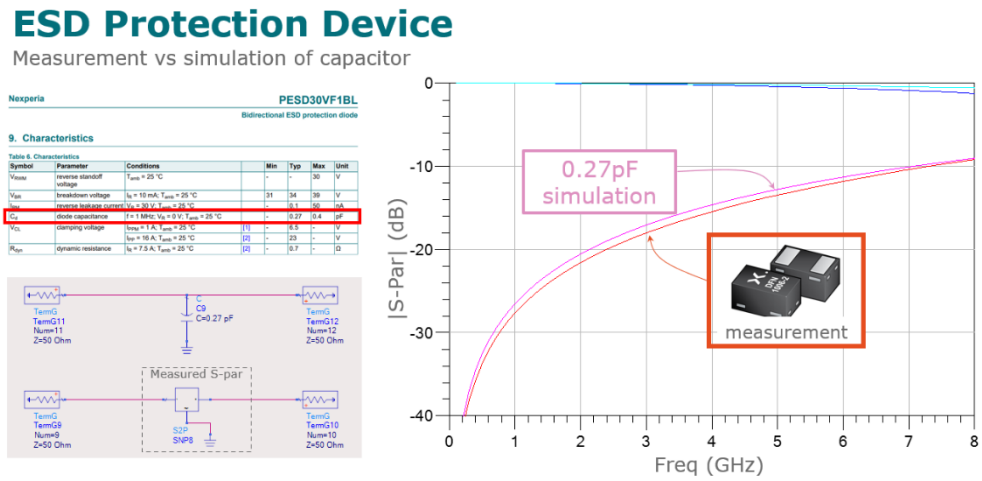
ESD for Electronic Design Engineers

Presentation no. 1 | Signal Integrity for ESD Protection Devices in Automotive High Speed Data Lines

Is the model of slide 10 spice, pspice or vhdl-ams and is the simulator ADS?



All simulations in this presentation were done in ADS.

For the capacitor simulation an ideal capacitor was assumed. The S-Parameter of the capacitor were compared with the measured S-Parameter of the real device. The comparison shows that the typical value of the device capacitance is a good value to use in a simulator. In addition, the parasitics of a modern compact package, in this case DFN1006 are not very dominant in this frequency range.

How about tolerances of the device capacitance? This could have strong impact on mode conversion for differential signaling

In general, this is true. The device capacitance of the ESD protections very low (<<1pF) and the absolute tolerance is also small. From this point of view, the impact should be not too strong. However, Nexperia plans to perform more investigations based on simulations and measurements to give quantitative results for the high-speed ESD protections devices in future. Please feel free to reach out to us on this topic to discuss the requirements and collaborate.

Can we simply compare s-parameter with our competitor? Or do we need to consider anything, such as conditions.

Throughout history, new ESD protection technologies were developed. First, people used large capacitors, Typically, the S-parameters are measured after carefully calibrating the Vector Network Analyzer (VNA) under lab conditions. Hence, the results should be comparable in general. But Nexperia cannot guarantee for the accuracy of the s-parameters from other companies.

Presentation no. 2 | Multi-component System-Efficient ESD Design (SEED) Simulation in Automotive Ethernet

Are the behavioural models of the ESD protection available? Do those models include parasitic parameters as shown in first presentation?

a. For transient analysis under ESD conditions we can offer behavioral dynamic SEED models generally in ADS but also in LTSpice possible.
b. For Signal Integrity simulations we can offer small-signal or RF optimized (also for certain devices HD optimized) LTSpice models.
c. All models can be prepared on your request, preparation time depends on complexity of the model and workload (estimated time will be provided then after request).

You showed CDM and HBM levels in your plot to show the safe area during system level events. Does this mean that you are only looking at un-powered IC conditions?
When powered, some chip-level ESD responses may be quite different from un-powered, e.g. those based on RC clamps.

a. For the system-level simulation (direct ESD discharge) shown in the presentation, we refer to the OPEN Alliance Specification for ESD Protection Devices, which defines this test to be done under unpowered condition.

b. In general, of course it is important to consider both scenarios since the IC internal protection technology can show different behaviors for powered/unpowered conditions.

c. However, in some cases the unpowered condition rather can represent the worst case scenario
(in powered mode Vdd helps to trigger ext. ESD protection device earlier and improve by that the overall system ESD robustness – best case scenario)

In regards of the second presentation, isn't required a 3D model of the ESD generator and test setup and PCB to better model the electric and magnetic fields and simulate the indirect coupling?

The idea of SEED is rather by investing comparably low effort (not possible, if we are talking about 3D models) to get to a system model, perform transient analysis, predict ESD robustness, optimize system parameters to improve the overall system ESD performance. The typical application scenario is direct ESD injection, but it is also possible to extend for indirect injection cases taking certain inaccuracy into account. That is still under further investigation.

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Presentation no. 2 | Multi-component System-Efficient ESD Design (SEED) Simulation in Automotive Ethernet

Have you ever simulated ESD Field Coupled test?

No. That is not in focus of SEED simulations we are doing

Can you please provide an overview on how to choose values of common mode choke, CMT and decaps? As you said <1pF is better approach for less losses on high-speed Ethernet

Please refer to the OPEN Alliance 100/1000Base-T1 ESD Device Test Specification: http://www.opensig.org/Automotive-Ethernet-Specifications/

Can I get a test report how you have implemented the measurements?

Please refer to the OPEN Alliance 100/1000Base-T1 ESD Device Test Specification: http://www.opensig.org/Automotive-Ethernet-Specifications/

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Presentation no. 3 | SEED Simulations of Powered Systems

What defines the typical limit for the internal IC protection diode failure? This is not something that most IC manufacturers include in their data sheets.

The IC IO protection is characterized by TLP of different pulse width. For thermal fail 50 ns TLP matches the IEC pulse best. In addition, 1.5 ns TLP is used to determined overvoltage fails due to fast transients. The failure criterion during TLP stepping is an increase of IO leakage. We additionally monitor the increase of IDDq on the supply line in the case of TLP under powered conditions. For a set of DUTs stressed below failure threshold of the leakage increase a full functional test is performed to ensure full functionality. All fail levels (It2/Vt at 50 ns and Vt2 at 5 ns) are incorporated into the SEED models. SEED models are not part of the datasheet, but are delivered as model set (similar to IBIS models etc). The way of delivery and the model format is actually different for different IC suppliers. The right contact is usual the customer field application engineer. ESDA WG26 is working on a standardized SEED model and model delivery.

You seem to assume that the PESD pulse that hits the IC has already been "stripped" of the initial PESD spike that happens with a much faster rise time (e.g. 500ps) and shorter pulse length (e.g. 2ns). If that spike came through to the IO, the external decoupling cap may have some non-negligible impedance in its board connections. Then the on-chip RC clamps may still be needed to protect VDD to VSS. How do you deal with this?

a. The RC clamp might need to turn on in the case of high impedance VDD supply nets a discussed. In the low impedance case the spike like the rest of the pulse is dumped into the caps of the IC and PCBs supply net. No turn-on of the RC power clamp will occur.
b. The initial spike at the IC pin is different to the Gun pulse spike, as it is a convolution of the incoming waveform, the turn-on behavior of the TVS diode and the filtering of the network between TVS diode and IC pin. In case of a fast and effective TVS diode turn-on and good filtering e.g. by CM chokes, no initial spike will be seen at the IC pin. This is the best design solution. However, for cases where an initial voltage overshoot occurs at the IC pin, the IC pin has to be characterized by vfTLP under powered conditions for hard fails. The RC power clamp can be a part of the ESD discharge path. The fail of the power clamp by vfTLP is monitored by IDDq measurement.
c. BTW: a triggering of a power clamp can also lead to soft fails.

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