



PSMN2R0-100SSF

NextPower 100 V, 2 mΩ, 259 Amp, N-channel MOSFET in LFPAK88 package

13 May 2020

Objective data sheet

1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 150 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 259 Amps $I_{D(max)}$ continuous current rating
- Low $Q_G \times R_{DS(on)}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK88 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch
- BLDC motor control
- Full-bridge and half-bridge applications
- Battery protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	259	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	284	W
T_j	junction temperature		-55	-	150	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 9	-	1.63	2.07	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 100\text{ °C}$; Fig. 10	-	2.6	3.3	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 11 ; Fig. 12	[tbd]	33.6	[tbd]	nC
$Q_{G(tot)}$	total gate charge		[tbd]	169	[tbd]	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 82\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	[1]	-	732	mJ

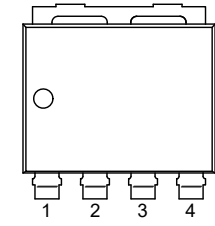
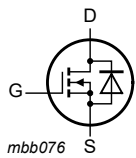
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q_r	recovered charge	$I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 50 \text{ V}$; Fig. 15	-	70	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LPAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-100SSF	LPAK88	plastic, single-ended surface-mounted package (LPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Limiting values

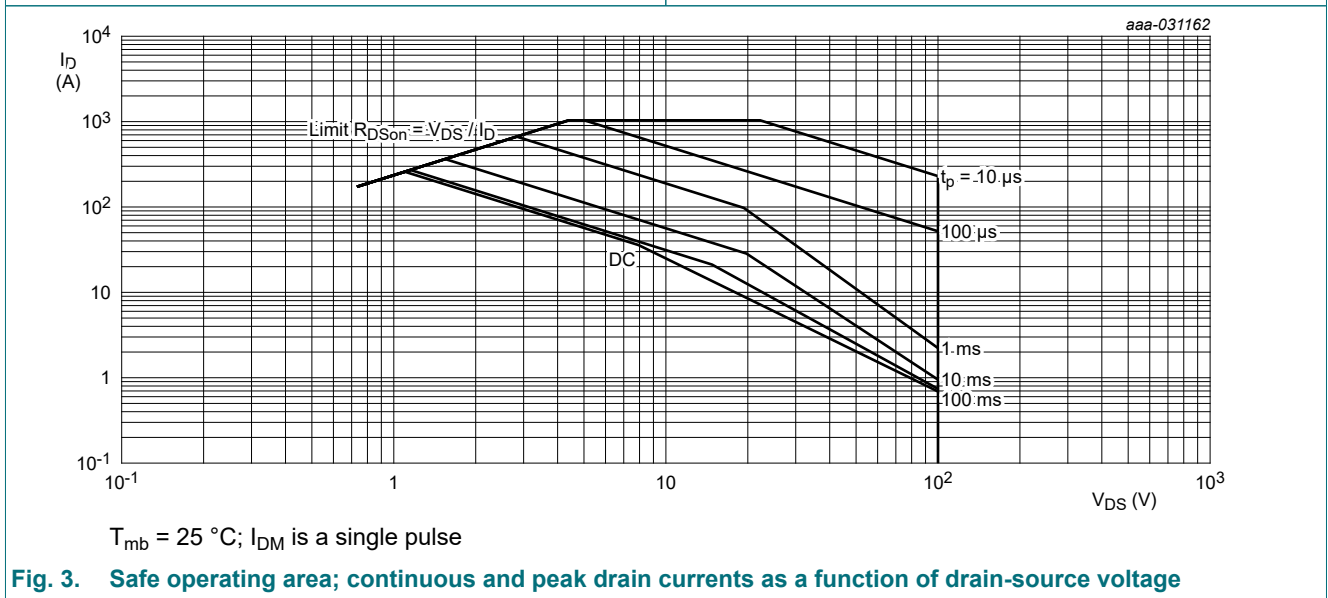
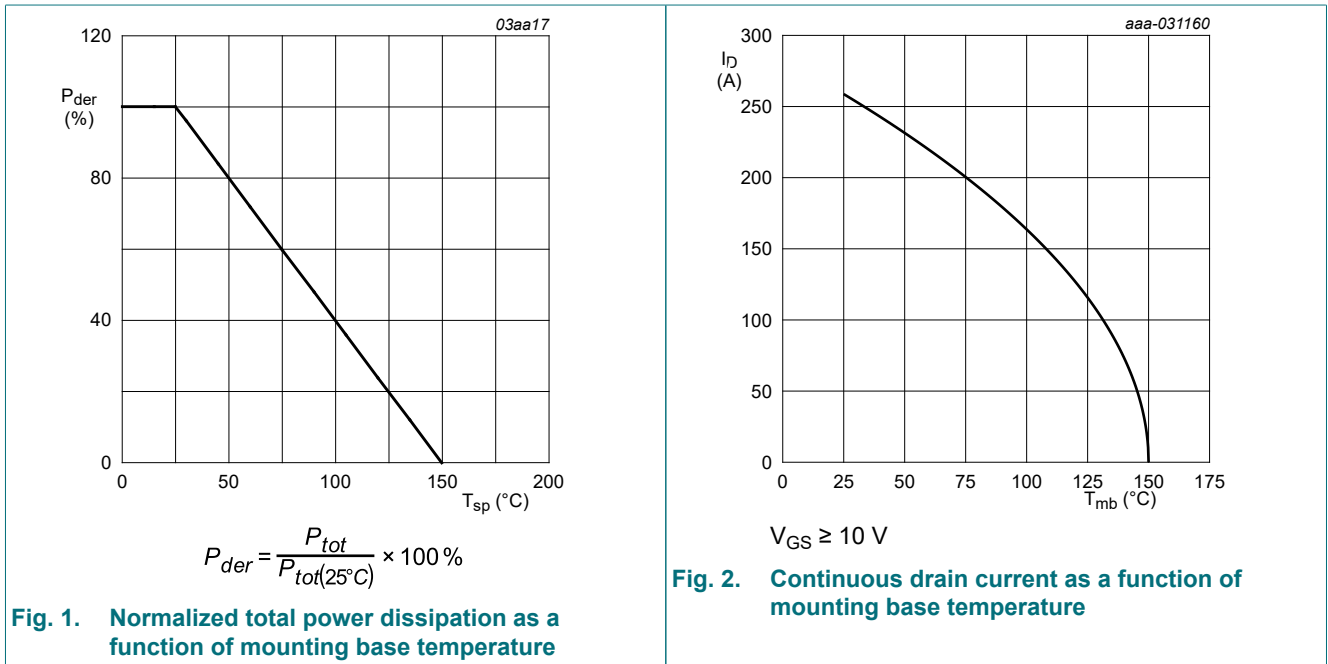
Table 4. Limiting values

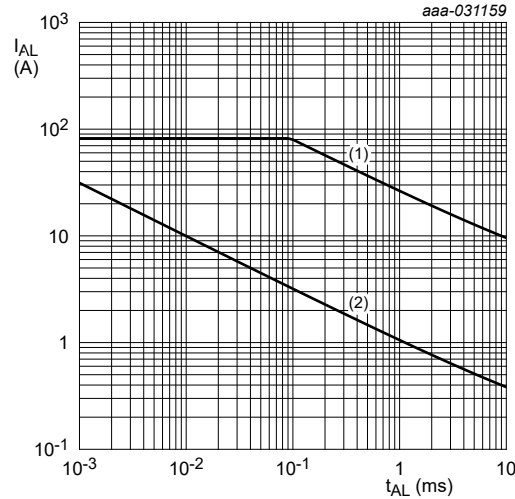
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25 \text{ °C} \leq T_j \leq 150 \text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$25 \text{ °C} \leq T_j \leq 150 \text{ °C}$; $R_{GS} = 20 \text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ °C}$; Fig. 1	-	284	W
I_D	drain current	$V_{GS} = 10 \text{ V}$; $T_{mb} = 25 \text{ °C}$; Fig. 2	-	259	A
		$V_{GS} = 10 \text{ V}$; $T_{mb} = 100 \text{ °C}$; Fig. 2	-	164	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25 \text{ °C}$; Fig. 3	-	1035	A
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25 \text{ °C}$	-	237	A
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25 \text{ °C}$	-	1035	A

Symbol	Parameter	Conditions	Min	Max	Unit	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 82 \text{ A}$; $V_{sup} \leq 100 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{J(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; Fig. 4	[1]	-	732	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 100 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_{J(\text{init})} = 25 \text{ }^\circ\text{C}$; $R_{GS} = 50 \Omega$; Fig. 4	[1]	-	82	A

[1] Protected by 100% test





(1) $T_{j\text{(init)}} = 25\text{ °C}$; (2) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	[tbd]	0.44	K/W

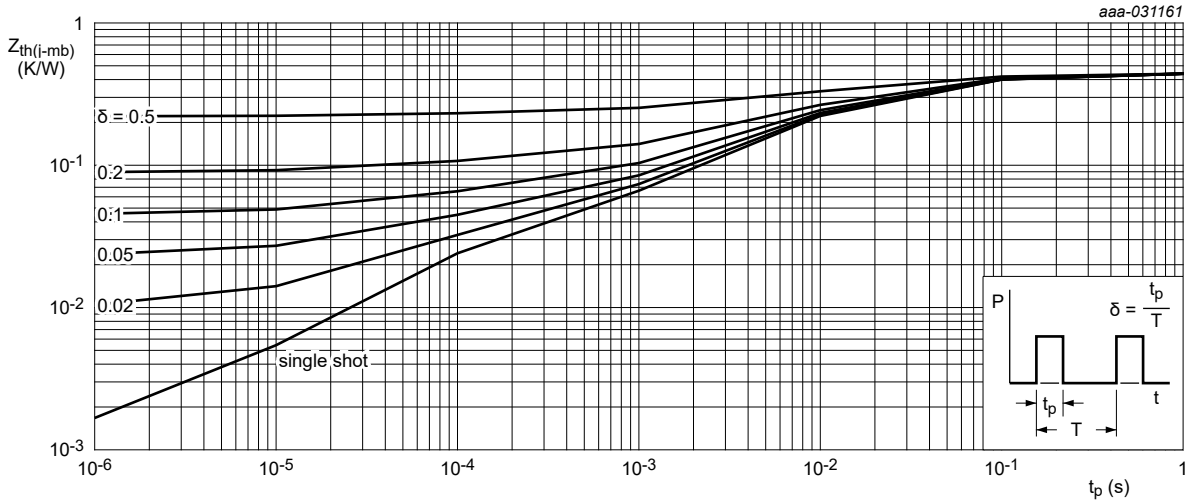


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	100	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ °C}$	90	-	-	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	3.5	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 150 \text{ }^\circ\text{C}$	-	1.9	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$	-	-8.4	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.1	25	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}; \text{ Fig. 9}$	-	1.63	2.07	mΩ
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}; \text{ Fig. 9}$	-	2	3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C}; \text{ Fig. 10}$	-	2.6	3.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ\text{C}; \text{ Fig. 10}$	-	3.3	4.2	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	[tbd]	1	[tbd]	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	[tbd]	169	[tbd]	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	-	87	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	[tbd]	48.7	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	32.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	16.4	-	nC
Q_{GD}	gate-drain charge		[tbd]	33.6	[tbd]	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	-	4.5	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}; \text{ Fig. 13}$	[tbd]	11764	[tbd]	pF
C_{oss}	output capacitance		[tbd]	2538	[tbd]	pF
C_{rss}	reverse transfer capacitance		[tbd]	88	[tbd]	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \text{ }^\circ\Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ }^\circ\Omega$	-	42	-	ns
t_r	rise time		-	35	-	ns
$t_{d(off)}$	turn-off delay time		-	103	-	ns
t_f	fall time		-	51	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{ Fig. 14}$	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; \text{ Fig. 15}$	-	58	-	ns
Q_r	recovered charge		-	70	-	nC

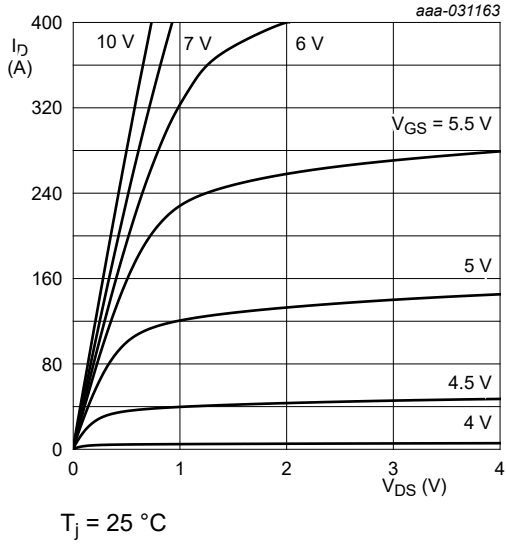


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

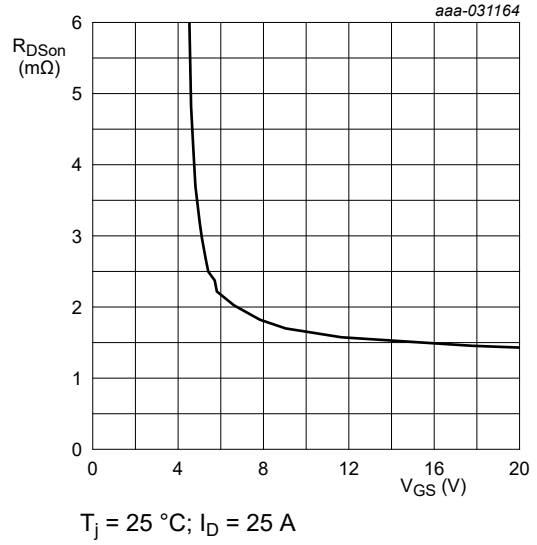


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

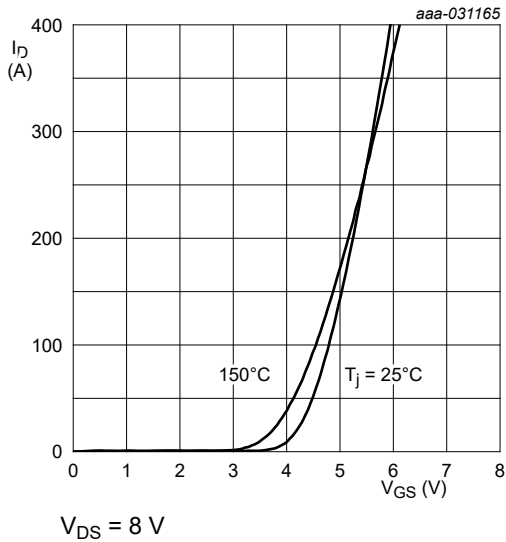


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

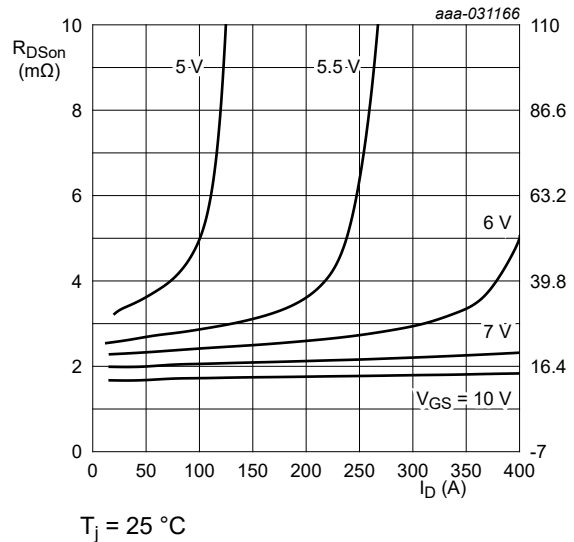
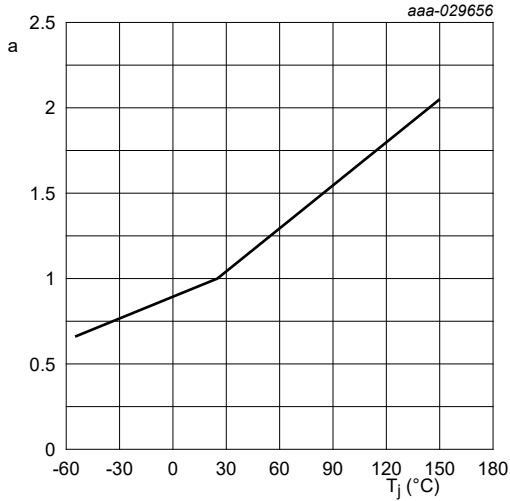
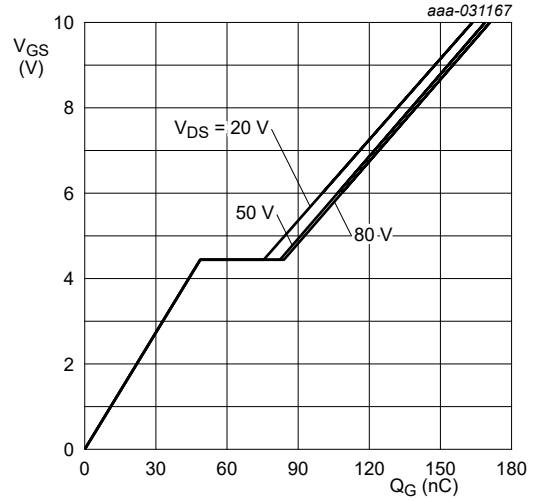


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon} (25^\circ\text{C})}$$

Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig. 11. Gate-source voltage as a function of gate charge; typical values

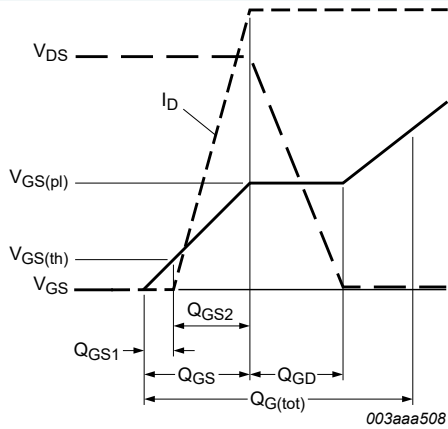
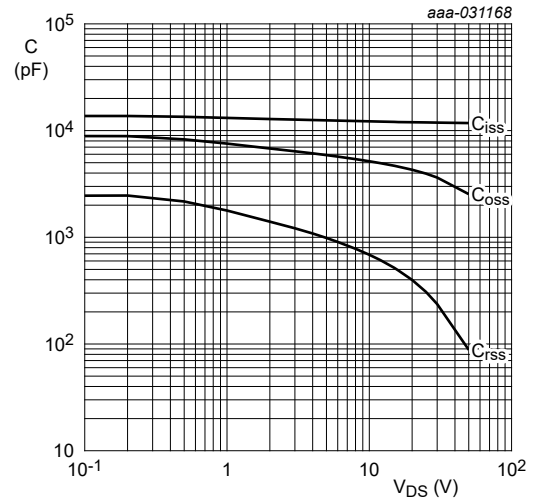


Fig. 12. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

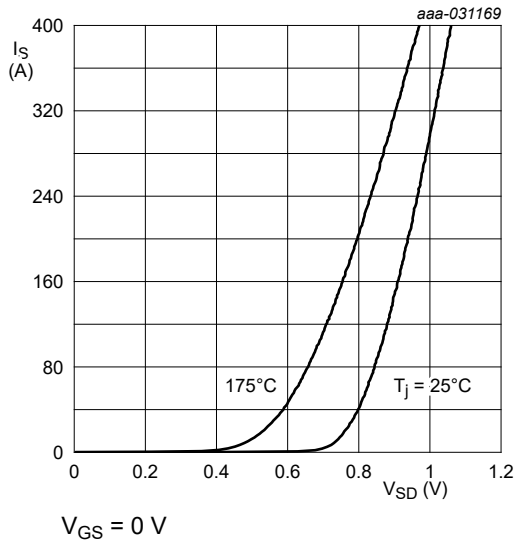


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

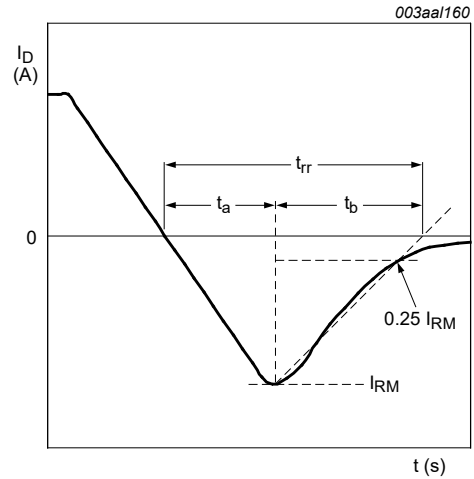


Fig. 15. Reverse recovery timing definition

10. Package outline

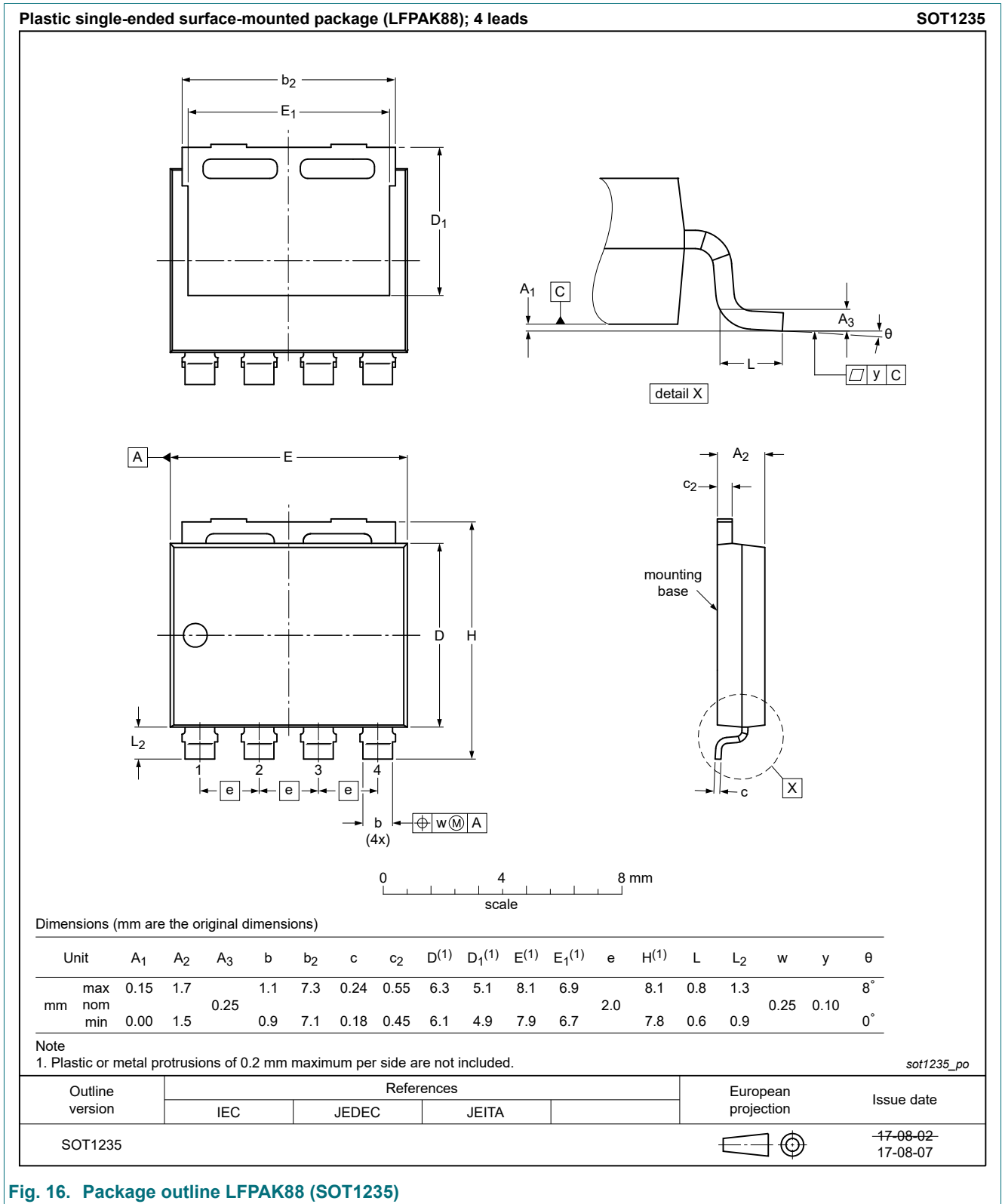


Fig. 16. Package outline LPAK88 (SOT1235)

11. Soldering

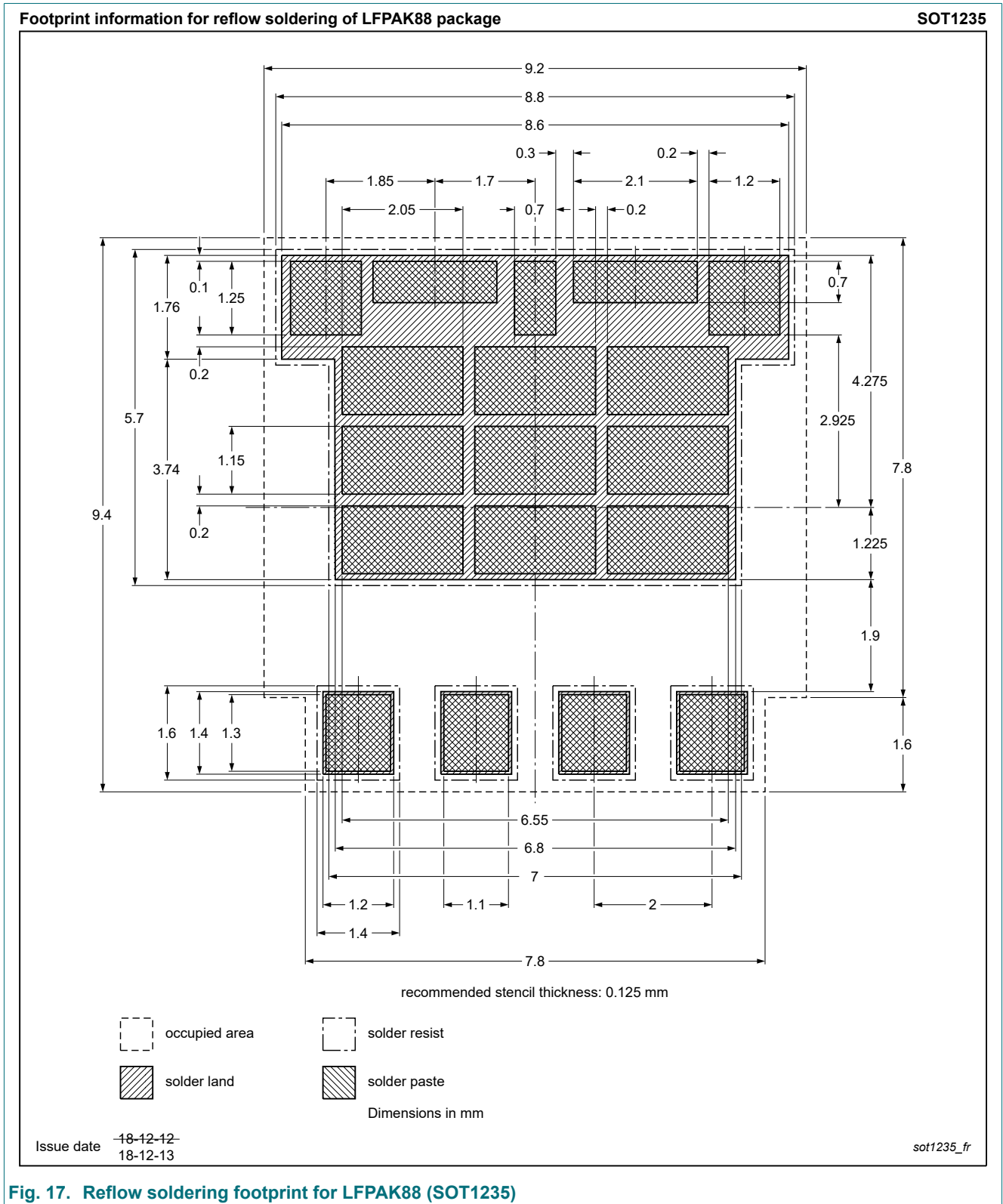


Fig. 17. Reflow soldering footprint for LPAK88 (SOT1235)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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