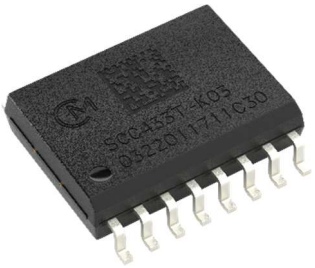
Data Sheet



SCC400T Series

SCR410T-K03 X gyroscope with digital SPI interface
SCC433T-K03 XZ gyroscope and XYZ accelerometer with digital SPI interface

Features

- ±300°/s X- or X/Z-axis angular rate measurement range
- ±6g 3-axis acceleration measurement range (XYZ, SCC433T-K03 only)
- ±8g 3-axis acceleration measurement range (XYZ, SCC433T-K03 only)
- −40°C…+110°C operating temperature range
- 3.0V…3.6V supply voltage
- SPI digital interface
- Extensive self-diagnostics features
- Housing body size 10.4 x 7.65 x 2.3 mm (l × w × h)
- RoHS compliant robust SOIC plastic package suitable for lead free soldering process and SMD mounting
- Proven capacitive 3D-MEMS technology

Applications

SCC400T series is targeted at applications demanding high stability with tough environmental requirements. Typical industrial applications include:

- Inertial Measurement Units (IMUs)
- Robotic control systems
- Machine control systems
- Platform stabilization and control
- Motion analysis and control

Restriction

- https://www.murata.com/en-global/support/militaryrestriction

Overview

SCC433T-K03 is a combined high performance angular rate and accelerometer sensor component based on Murata's proven capacitive 3D-MEMS technology. Signal processing is done in one mixed signal ASIC that provides angular rate and acceleration output via flexible SPI digital interface. Sensor elements and ASIC are packaged to overmolded SOIC-16W plastic housing that guarantees reliable operation over product's lifetime.

SCR410T-K03 is a high performance angular rate sensor component based on the same technology, housing and SPI digital interface as SCC433T-K03.

SCC433T-K03 and SCR410T-K03 are designed, manufactured and tested for high stability, reliability and quality requirements. Components have extremely stable output over temperature, humidity and vibration. Components have several advanced self-diagnostic features and it is suitable for SMD mounting and is compatible with RoHS and ELV directives.

1 Introduction

This document contains essential technical information related to all SCC400T series sensors including specifications, SPI interface descriptions, user accessible register details, electrical properties and application information. This document together with the document "APP 10207 Assembly instructions for SCC400T Series" should be used as a reference when designing in SCC400T series component. All content of this document is not valid for all product versions, please see below for register and functionality validity.

Table 1. Register and functionality validity for SCC400T series product versions.

	SCC433T-K03	SCR410T-K03
X-gyro functionality (±300°/s)	☒	☒
Z-gyro functionality (±300°/s)	☒	☐
ACC functionality (±6g)	☒	☐
ACC LGS functionality (±8g)	☒	☐
Temperature sensing functionality	☒	☒

2 Specifications

This chapter includes all specifications, typical performance and general information for SCC400T series.

2.1 Abbreviations

ASIC	Application Specific Integrated Circuit
SPI	Serial Peripheral Interface
RT	Room Temperature
DPS	Degrees per second
FS	Full scale
OS	Out of specification
CSB	Chip Select
SCK	Serial Clock
MOSI	Master Out Slave In
MISO	Master In Slave Out
MCU	Microcontroller
LGS	Secondary accelerometer output
BIST	Built-in Self test
DSP	Digital Signal Processor
CCM	Channel calibration and monitoring
Rx	Rate X axis
Rz	Rate Z axis
Ax	Accelerometer X axis
Ay	Accelerometer Y axis
Az	Accelerometer Z axis
F_prim	Nominal operation frequency of the sensor element
DOF	Degrees of Freedom

2.2 Performance Specifications for Gyroscope

Table 2.Performance specifications with VDD = 3.3 V and at room temperature (RT) unless otherwise specified.

Parameter	Condition	Unit	SCC400T series SCC433T-K03 and SCR410T-K03			
			Axis	Min *	Typ *	Max *
Operating temperature range **		°C	X/Z	-40		110
Measurement range **		°/s	X/Z	-300		300
Total offset error	-40 °C ... +110 °C	°/s	X	-1.2		1.2
			Z	-0.7		0.7
Offset drift over lifetime ***	After HTOL 1000h	°/s	X	-0.9		0.9
			Z	-0.4		0.4
Offset drift over temperature	-40 °C ... +110 °C	°/s	X	0		0.8
			Z	0		0.4
Offset drift velocity	2.5K /min, -40 °C ... +110 °C	°/s / min	X	-0.1		0.1
			Z	-0.05		0.05
Sensitivity	Target value	LSB/°/s	X/Z		80	
Total sensitivity error (lifetime)	-40 °C ... +110 °C	%	X	-3		3
			Z	-1		1
Linearity error	-300dps ... +300dps, -40 °C ... +110 °C	°/s	X	-0.5		0.5
			Z	-0.4		0.4
	-250dps ... +250dps, -40 °C ... +110 °C	°/s	X	-0.4		0.4
			Z	-0.3		0.3
Noise (RMS)	13 Hz filter, -40 °C ... +110 °C	°/s	X/Z		0.009	0.014
	20 Hz filter, -40 °C ... +110 °C	°/s	X/Z		0.011	0.017
	46 Hz filter, -40 °C ... +110 °C	°/s	X/Z		0.015	0.025
	200Hz filter, -40 °C ... +110 °C	°/s	X/Z		0.1	0.15
	200Hz filter, -40 °C ... +110 °C Gyro CST disabled	°/s	X/Z		0.05	0.1
	300Hz filter, -40 °C ... +110 °C	°/s	X/Z		0.05	0.1
Noise density	-40 °C ... +110 °C	°/s/√Hz	X/Z		0.002	
Angle Random Walk		°/√h	X/Z		0.09	
Bias Instability	Allan Variance minimum	°/h	X		1.3	
			Z		1.1	
	Allan Variance minimum divided by 0.664	°/h	X		1.9	
			Z		1.6	
Cross-axis sensitivity	-40 °C ... +110 °C	%	X/Z	-1.5		1.5
Amplitude response −3 dB frequency	13 Hz filter	Hz	X/Z		13	
	20 Hz filter	Hz	X/Z		20	
	46 Hz filter	Hz	X/Z		46	
	200 Hz filter	Hz	X/Z		219	
	300 Hz filter	Hz	X/Z		299	
Power on start-up time **	13, 20 Hz filter (after SPI power on command)	ms	X/Z			620
	46, 200, 300 Hz filter (after SPI power on command)	ms	X/Z			500
F_prim ** Nominal operation frequency of the sensor element. All ASIC internal clocks are derived from a multiple of this frequency		kHz	X	15.8	16.8	17.8
			Z	18.3	19.3	20.3
Electrical Dynamic Range (Headroom)	Output signal	°/s	X/Z		±409.6	
Output update rate		kHz	X/Z		F_prim/2	
G sensitivity (1g x,y,z axis)	DC gravity input	(°/s)/G	X/Z	-0.01		0.01

* Specified Min/Max values contain ±3 sigma variation limits of original test population. Typical values are validation population mean (unless otherwise specified). Min/Max and typical values are not guaranteed, values represent validation population characteristics.
** Guaranteed value
*** Min/max values are example of original test population ±3 sigma limits, values not guaranteed.

Note :
• Specification is valid after 24hours from reflow.
• Each system design including SCC400T series component must be evaluated by the customer in advance to guarantee proper functionality during operation.

Table 3. Gyroscope parameter definitions

Parameter	Description
Total offset error	Includes offset error from calibration, temperature, supply voltage and drift over lifetime. Lifetime tests include following tests listed in AEC-Q100: TC, HTSL, HTOL, HBM, CDM, LU, MS, VFV, CA, DROP. Statistical mean and ±3sigma is evaluated only for tests with N ≥ 30pcs.
Offset drift over lifetime	Offset change in room temperature (RT) during HTOL test, offset zeroed to initial measurement, N ≥ 90pcs HTOL: 1000 hours of high temperature operating life at +125°C, VDD=3.6V.
Offset drift over temperature	Offset drift over temperature is determined by ((maximum offset value over temperature) - (minimum offset value over temperature)) / 2 in condition of one temperature sweep in specified temperature range.
Sensitivity	Sensitivity is defined as $Sensitivity = \frac{AR_{meas}(\Omega_{max}) - AR_{meas}(\Omega_{min})}{\Omega_{max} - \Omega_{min}}$ Where Ω_{max}=applied angular rate at maximum operating range Ω_{min}=applied angular rate at minimum operating range $AR_{meas}(\Omega_n)$ = measured angular rate at Ω_n [LSB]
Total sensitivity error	Includes sensitivity error from calibration, temperature, supply voltage and drift over lifetime. Lifetime tests listed in total offset error.
Linearity error	Linearity is the maximum deviation from the straight line defined by the measured values at the operating range endpoints.
Cross-axis sensitivity	Cross axis sensitivity is the ratio between the sensitivity of the sensing axis and the two orthogonal axes. Xgyro product version： $Cross\ axis\ (Y) = \frac{Sensitivity(Y)}{Sensitivity(X)} \times 100\%, Cross\ axis\ (Z) = \frac{Sensitivity(Z)}{Sensitivity(X)} \times 100\%$ Zgyro product version： $Cross\ axis\ (X) = \frac{Sensitivity(X)}{Sensitivity(Z)} \times 100\%, Cross\ axis\ (Y) = \frac{Sensitivity(Y)}{Sensitivity(Z)} \times 100\%$ Where Sensitivity(X)= Sensitivity when angular rate is applied in X direction Sensitivity(Y)= Sensitivity when angular rate is applied in Y direction Sensitivity(Z)=Sensitivity when angular rate is applied in Z direction

2.3 Performance Specifications for Accelerometer

Table 4. Performance specifications with VDD = 3.3 V and at room temperature unless otherwise specified.

Parameter	Condition	Unit	SCC400T series SCC433T-K03			
			Axis	Min *	Typ *	Max *
Operating temperature range **		°C	X/Y/Z	-40		110
Measurement range **		g	X/Y/Z	-6		6
Total Offset error	-40 °C ... +110 °C	mg	X/Y	-25		25
			Z	-45		45
Offset drift over lifetime ***	In RT, after HTOL 1000h	mg	X/Y	-17		17
			Z	-25		25
Offset drift over temperature	-40 °C ... +110 °C	mg	X/Y	0		15
			Z	0		20
Offset drift velocity	2.5K /min, -40 °C ... +85 °C	mg / min	X/Y/Z	-3		3
	2.5K /min, -40 °C ... +110 °C	mg / min	X/Y/Z	-6		6
Sensitivity	Target value	LSB/g	X/Y/Z		4905	
Total sensitivity error	−1 g …1 g range, -40 °C ... +110 °C	%	X/Y	-0.5		0.5
			Z	-0.6		0.6
Linearity error	−1 g …1 g range	mg	X/Y/Z	-1		1
	−1 g …1 g range, -40 °C ... +110 °C	mg	X/Y/Z	-5		5
	−6 g …6 g range, -40 °C ... +110 °C	mg	X/Y	-30		30
			Z	-45		45
Cross-Axis sensitivity	per axis	%	X/Y/Z	-1.5		1.5
Noise (RMS)	13 Hz filter, -40 °C ... +110 °C	mg	X/Y/Z		0.35	0.5
	20 Hz filter, -40 °C ... +110 °C	mg	X/Y/Z		0.4	0.7
	46 Hz filter, -40 °C ... +110 °C	mg	X/Y/Z		0.6	0.8
	200Hz filter, -40 °C ... +110 °C	mg	X/Y/Z		1.5	4
	300Hz filter, -40 °C ... +110 °C	mg	X/Y/Z		2	5
Noise density	-40 °C ... +110 °C	$\mu g/\sqrt{Hz}$	X/Y/Z		70	
Amplitude response −3 dB frequency	13 Hz filter	Hz	X/Y		13	
	20 Hz filter	Hz	X/Y		20	
	46 Hz filter	Hz	X/Y		46	
	200 Hz filter	Hz	X/Y		198	
	300 Hz filter	Hz	X/Y		251	
	13 Hz filter	Hz	Z		13	
	20 Hz filter	Hz	Z		20	
	46 Hz filter	Hz	Z		46	
	200 Hz filter	Hz	Z		208	
	300 Hz filter	Hz	Z		272	
Power on start-up time **	13, 20 Hz filter (after SPI power on command)	ms	X/Y/Z			450
	46, 200, 300 Hz filter (after SPI power on command)	ms	X/Y/Z			320
Electrical Dynamic Range (Headroom)		g	X/Y/Z		±6.7	
Output update rate	Accelerometer: X-gyro F_prim	kHz	X/Y/Z		F_prim/2	

* Specified Min/Max values contain ±3 sigma variation limits of original test population. Typical values are validation population mean (unless otherwise specified). Min/Max and typical values are not guaranteed, values represent validation population characteristics.

** Guaranteed value

*** Example of test population ±3 sigma limits, values not guaranteed.

Note :

- Specification is valid after 24hours from reflow.
- Each system design including SCC400T series component must be evaluated by the customer in advance to guarantee proper functionality during operation.

2.4 Performance Specifications for Secondary Accelerometer Output

Table 5. Performance specifications with VDD = 3.3 V and at room temperature unless otherwise specified.

Parameter	Condition	Unit	SCC400T series SCC433T-K03			
			Axis	Min *	Typ *	Max *
Operating temperature range **		°C	X/Y/Z	-40		110
Measurement range **		g	X/Y/Z	-8		8
Total Offset error	-40 °C ... +110 °C	mg	X/Y	-25		25
			Z	-45		45
Offset drift over temperature	-40 °C ... +110 °C	mg	X/Y	0		15
			Z	0		20
Sensitivity	Target value	LSB/g	X/Y/Z		2452.5	
Total sensitivity error	−1 g …1 g range, -40 °C ... +110 °C	%	X/Y	-0.5		0.5
			Z	-0.6		0.6
Linearity error	−1 g …1 g range	mg	X/Y/Z	-1		1
	−1 g …1 g range, -40 °C ... +110 °C	mg	X/Y/Z	-5		5
	−8 g …8 g range, -40 °C ... +110 °C	mg	X/Y	-50		50
			Z	-100		100
Cross-Axis sensitivity	per axis	%	X/Y/Z	-1.5		1.5
Noise (RMS)	200Hz filter, -40 °C ... +110 °C	mg RMS	X/Y/Z		1.5	4
	300Hz filter, -40 °C ... +110 °C	mg RMS	X/Y/Z		2	5
Amplitude response −3 dB frequency	200 Hz filter	Hz	X/Y		198	
	300 Hz filter	Hz	X/Y		251	
	200 Hz filter	Hz	Z		208	
	300 Hz filter	Hz	Z		272	
Output update rate	Accelerometer: X-gyro F_prim	kHz	X/Y/Z		16× F_prim	

* Specified Min/Max values contain ±3 sigma variation limits of original test population. Typical values are validation population mean (unless otherwise specified). Min/Max and typical values are not guaranteed, values represent validation population characteristics.

** Guaranteed value

Note :

• Specification is valid after 24hours from reflow.

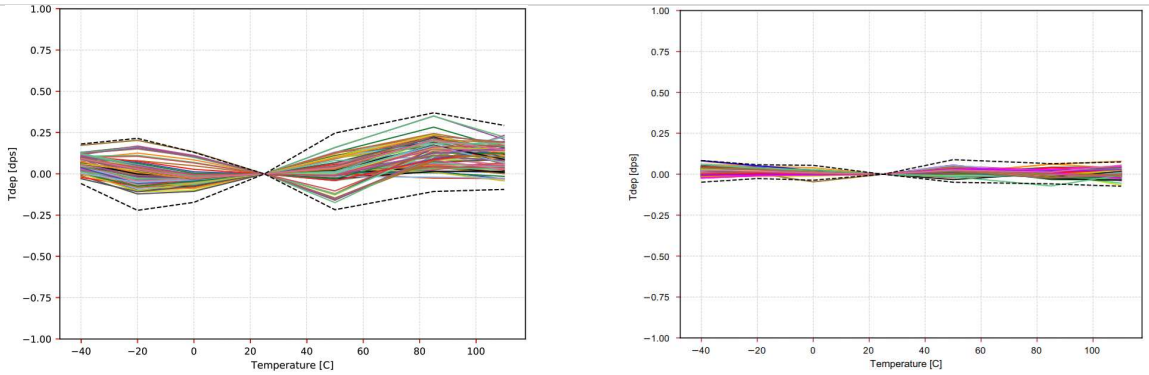
• Each system design including SCC400T series component must be evaluated by the customer in advance to guarantee proper functionality during operation.

Table 6. Accelerometer and secondary accelerometer parameter definitions

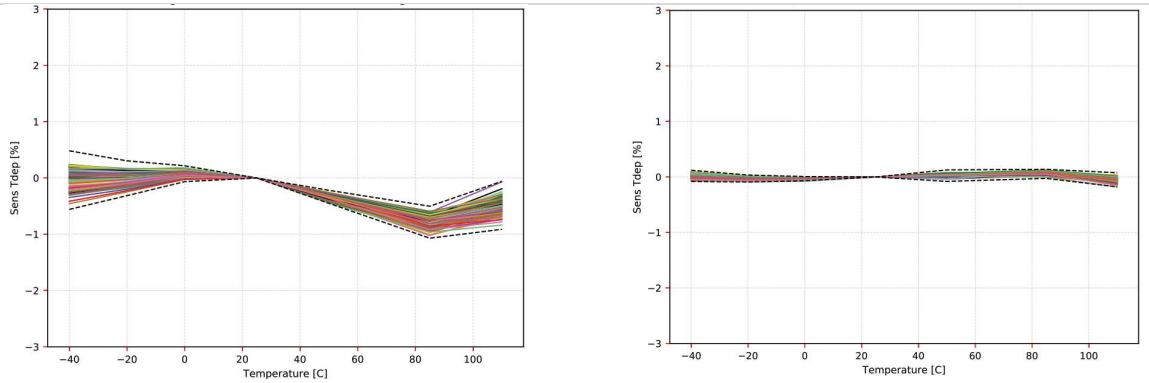
Parameter	Description
Total Offset error	Includes offset error from calibration, temperature, supply voltage and drift over lifetime. Lifetime tests include following tests listed in AEC-Q100: TC, HTSL, HTOL, HBM, CDM, LU, MS, VFV, CA, DROP. Statistical mean and ±3sigma is evaluated only for tests with N ≥ 30pcs.
Offset drift over lifetime	Offset change in room temperature (RT) during HTOL test, offset zeroed to initial measurement, N ≥ 90pcs HTOL: 1000 hours of high temperature operating life at +125°C, VDD=3.6V.
Offset drift over temperature	Offset drift over temperature is determined by ((maximum offset over temperature) - (minimum offset over temperature)) / 2 in condition of one temperature sweep in specified temperature range.
Sensitivity	Sensitivity is defined as $Sensitivity = \frac{ACC_{meas}(a_{+1g}) - ACC_{meas}(a_{-1g})}{a_{+1g} - a_{-1g}}$ Where a_{+1g}=applied acceleration at +1g (i.e. +1g gravity of manufacturing location) a_{-1g}=applied acceleration at -1g (i.e. -1g gravity of manufacturing location) $ACC_{meas}(a_n)$=measured acceleration at a_n [LSB]
Total sensitivity error	Includes sensitivity error from calibration, temperature, supply voltage and drift over lifetime. Lifetime tests listed in total offset error.
Linearity error	Linearity is the maximum deviation from the straight line defined by the measured values at the operating range end points.
Cross-Axis sensitivity	Cross-axis sensitivity is the maximum sensitivity in the plane perpendicular to the measuring direction relative to the sensitivity in the measuring direction. $Cross - axis\_sensitivity = \frac{ACC_{meas} - ACC_{meas2}}{2 \times Sensitivity} \times 100\%$ Where ACC_{meas}= measured acceleration in 0g position perpendicular to the measuring direction

2.5 Gyro typical performance characteristics for SCC400T series

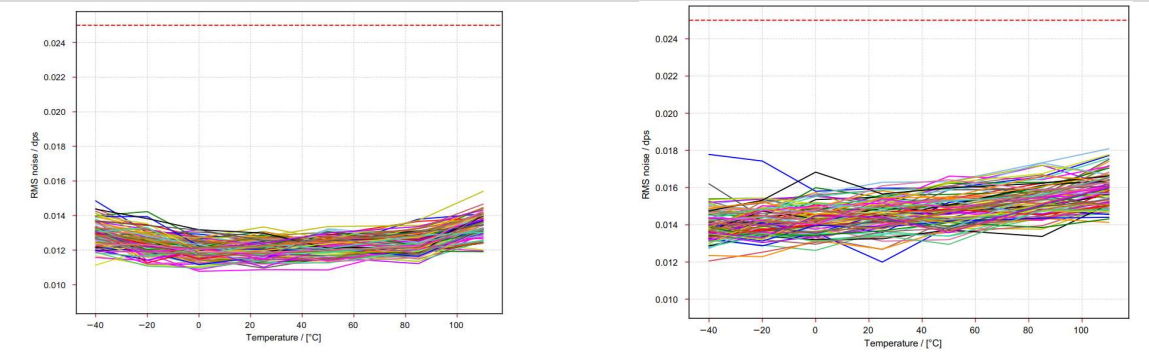
X-Gyro **Z-Gyro**



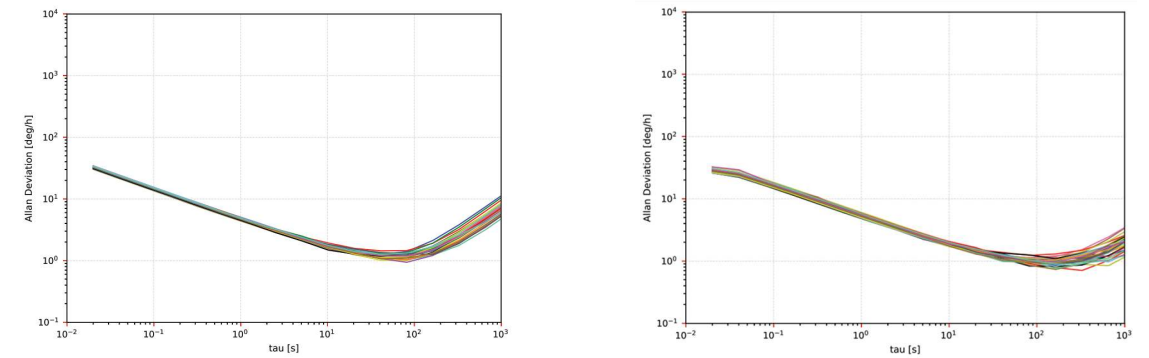
Offset drift over temperature from room temperature (°/s)



Sensitivity drift over temperature from room temperature (%)



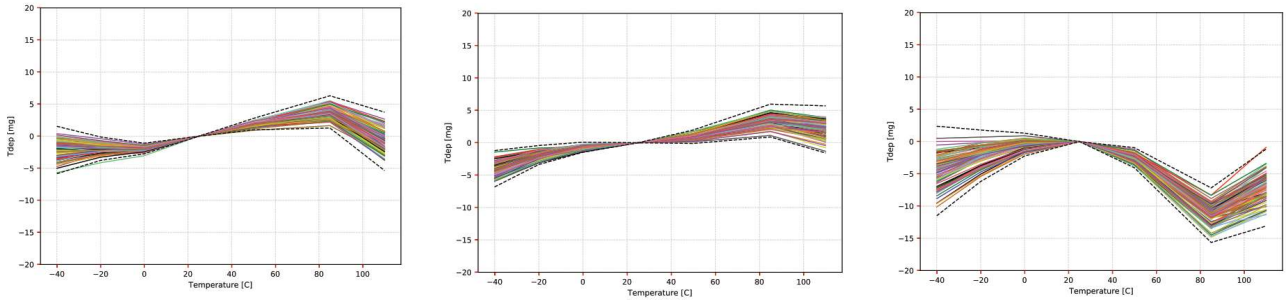
RMS noise 46Hz LPF (°/sRMS)



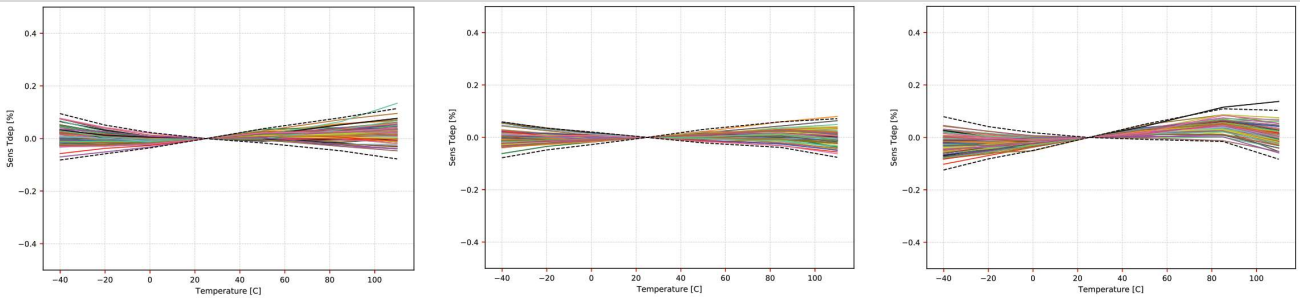
Allan variance

2.6 Accelerometer typical performance characteristics for SCC433T-K03 series

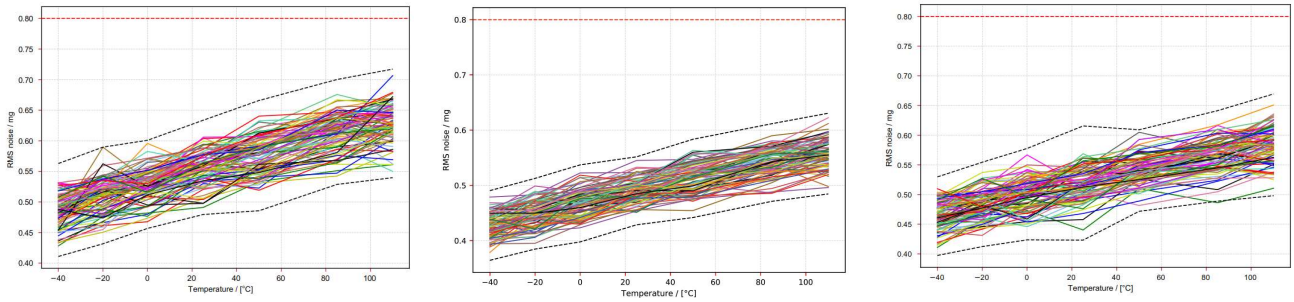
ACC_X	ACC_Y	ACC_Z



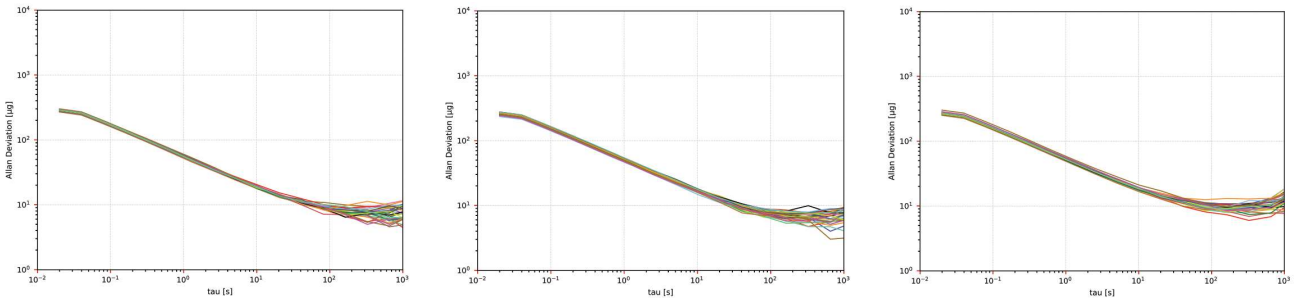
Offset drift over temperature from room temperature (mg)



Sensitivity drift over temperature from room temperature (%)



RMS noise 46Hz LPF (mgRMS)



Allan variance

2.7 General Specifications

General specifications for SCC400T series component are presented in Table 7. All analog voltages are related to the potential at GNDA and all digital voltages are related to the potential at GNDD.

Table 7. General specifications.

Parameter	Condition		CC/ SC	Unit	Min	Typ	Max
Supply voltage: V3p3A	Analog supply Voltage			V	3.0	3.3	3.6
Supply voltage: V3p3D	Digital supply voltage			V	3.0	3.3	3.6
Total current, I_TOTAL	Total current consumption during normal operation mode I_TOTAL= Analog + Digital supply current	1DOF	CC	mA		12	19
		5DOF	CC	mA		19	25
Total current, I_TOTAL	In lower power mode (Before operation mode on)			mA		3	5
Total current reset	Total average current during reset			mA			2
POR_TH_H	Threshold of Power On Reset (POR) for rising V3p3A, V3p3D			V	2.7	2.8	2.9
POR_TH_L	Threshold of Power On Reset (POR) for falling V3p3A, V3p3D			V	2.5	2.6	2.8
TRESD_r	Time to reset delay for rising inputs Wait time that rising supply voltages and rising EXTRESN input signal (optional) are above their threshold levels.			ms	15		
TMODE	Wait time to set the operation mode after the supply in the specification. Wait time needed after power on or after reset. (Wait time starts when supply is inside spec limits.) SPI is not functional during this time.			ms	25		
TRES_SPI	Time to reset SPI : Wait time after reset. CSB shall be high.			ms	2		

2.8 Performance Specification for Temperature Sensor

Table 8. Temperature sensor performance specifications.

Parameter	Condition	Min.	Typ	Max.	Unit
Temperature signal range		-50		+149	°C
Temperature signal sensitivity			30		LSB/°C
Offset error		-15		+15	°C
Sensitivity error		-10		+10	%
Linearity error			±3		%

Temperature is converted to °C with following equation: Temperature [°C] = 25 + (TEMP / 30) where TEMP is temperature sensor output register content in decimal format (2's complement).

2.9 Absolute Maximum Ratings

Within the maximum ratings (Table 9. Absolute maximum ratings.) in an instant, no damage to the component shall occur. Parametric values may deviate from specification, yet no functional deviation shall occur. All analog voltages are related to the potential at GNDA, all digital voltages are related to GNDD.

Table 9. Absolute maximum ratings.

Parameter	Remark	Min.	Recommended	Max.	Unit
SUPPLY	Supply voltage (pins V3p3A, V3p3D)	-0.3		4.3	V
AIN/AOUT	Voltage at analog input and output pins	-0.3		SUPPLY+0.3 ≤4.3	V
DIN/DOUT	Voltage at digital input and output pins	-0.3		SUPPLY+0.3 ≤4.3	V
Tstg	Storage temperature range A)	-50		140	°C
ESD_HBM	ESD according Human Body Model (HBM), Q100-002	-2000		2000	V
ESD_MM	ESD according Machine Model (MM), Q100-003	-200		200	V
ESD_CDM	ESD according Charged Device Model (CDM), Q100-011	-500 -750 (corner pins)		500 750 (corner pins)	V
-	Max peak body temperature during reflow B)			260	°C
-	Maximum storage time before soldering		1	2	years
US	Ultrasonic agitation (cleaning, welding, etc)	Prohibited			

A) No damage to the component shall occur within the maximum ratings in an instant and also max 24hour,

B) Maximum allowable time within 260°C +0°C/-5°C = 30s.

2.10 Pin Description

The pinout for SCC400T is presented in Figure 1, while the pin descriptions can be found in Table 10.

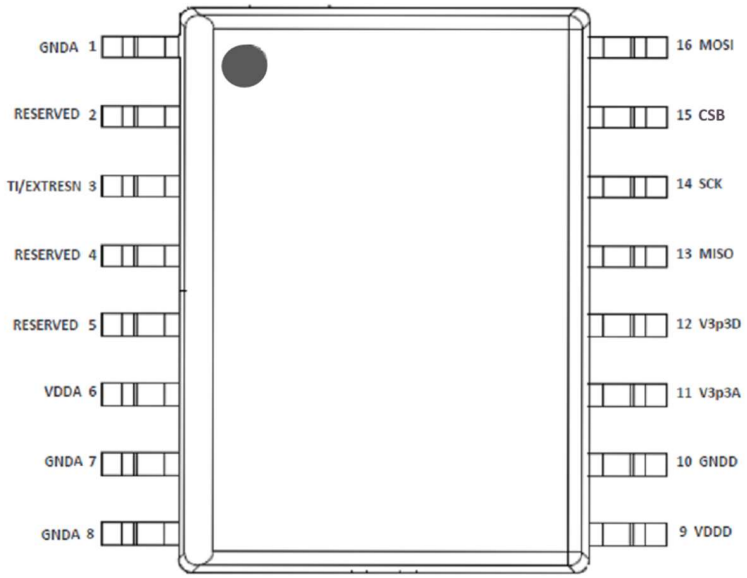


Figure 1. Pinout for SCC400T.

Table 10. SCC400T pin descriptions.

Pin#	Name	Type	Description
1	GNDA	GND	EMC protection and ground
2	RESERVED	-	Factory use only, connect to GND
3	TI/EXTRESN	DIN	Optional external Reset, 3.3V logic compatible Schmitt-trigger input with internal pull-up, LOW-HIGH transition causes system restart. Minimum low time 100us.
4	RESERVED	-	Factory use only, connect to GND
5	RESERVED	-	Factory use only, connect to GND
6	VDDA	AOUT	Regulated supply for analog core. Use external capacitor which is connected according to the diagram in Figure 18.
7	GNDA	GND	Analog Supply return (ground), connect externally to GND
8	GNDA	GND	Analog Supply return (ground), connect externally to GND
9	VDDD	AOUT	Regulated supply for digital core. Use external capacitor which is connected according to the diagram in Figure 18.
10	GNDD	GND	Digital Supply return (ground), connect externally to GND
11	V3p3A	SUPPLY	Analog Supply voltage
12	V3p3D	SUPPLY	Digital Supply voltage
13	MISO	DOUT	Data Out of SPI Interface
14	SCK	DIN	Clock Signal of SPI Interface
15	CSB	DIN	Chip Selected of SPI Interface
16	MOSI	DIN	Data In of SPI Interface

2.11 Digital I/O Specification

Table 11 describes the DC characteristics of SCC400T sensor SPI I/O pins. Supply voltage is 3.3 V unless otherwise specified. Current flowing into the circuit has a positive value.

Table 11. SPI DC characteristics.

Symbol	Description	Min.	Nom.	Max.	Unit
Serial Clock SCLK					
VinHigh	Input high voltage	2		V3p3D+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.2			V
Isource	Input current source (Pull down) , Vin = DVDD	24		36	uA
Cin	Input capacitance			6	pF
Chip select CSB (Pull Up), low active					
VinHigh	Input high voltage	2		V3p3D+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.2			V
Isource	Input current source (Pull Up), Vin = 0V	24		36	uA
Cin	Input capacitance			6	pF
Vin_open	Open circuit output voltage	2			V
Serial data input MOSI (Pull Down)					
VinHigh	Input high voltage	2		V3p3D+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.2			V
Isource	Input current source (Pull Up), Vin = DVDD	24		36	uA
Cin	Input capacitance			6	pF
Vin_open	Open circuit output voltage			0.3	V
Serial data output MISO (Tri state)					
VoutHigh_-1mA	Output high voltage, Iout = -1mA	V3p3D-0.5			V
VinHigh_1mA	Output low voltage, Iout = +1mA			0.5	V
Iout_Hz	High impedance output current, 0V < VMISO < V3p3D	-1		1	uA
Cld_miso	Capacitive load. The slope of the MISO output signal can be controlled to meet EMI requirements under specified load conditions.			160	pF

Table 12. EXTRESN pin characteristics

Symbol	Description	Min.	Nom.	Max.	Unit
Digital pin EXTRESN					
VinHigh	Input high voltage	2		V3p3A+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.2			V
Isource	Start-up indication phase inactive Start-up indication phase active	60 30		160 80	µA µA

2.12 SPI AC Characteristics

The AC characteristics of SCC400T are defined in Figure 2 and Table 13.

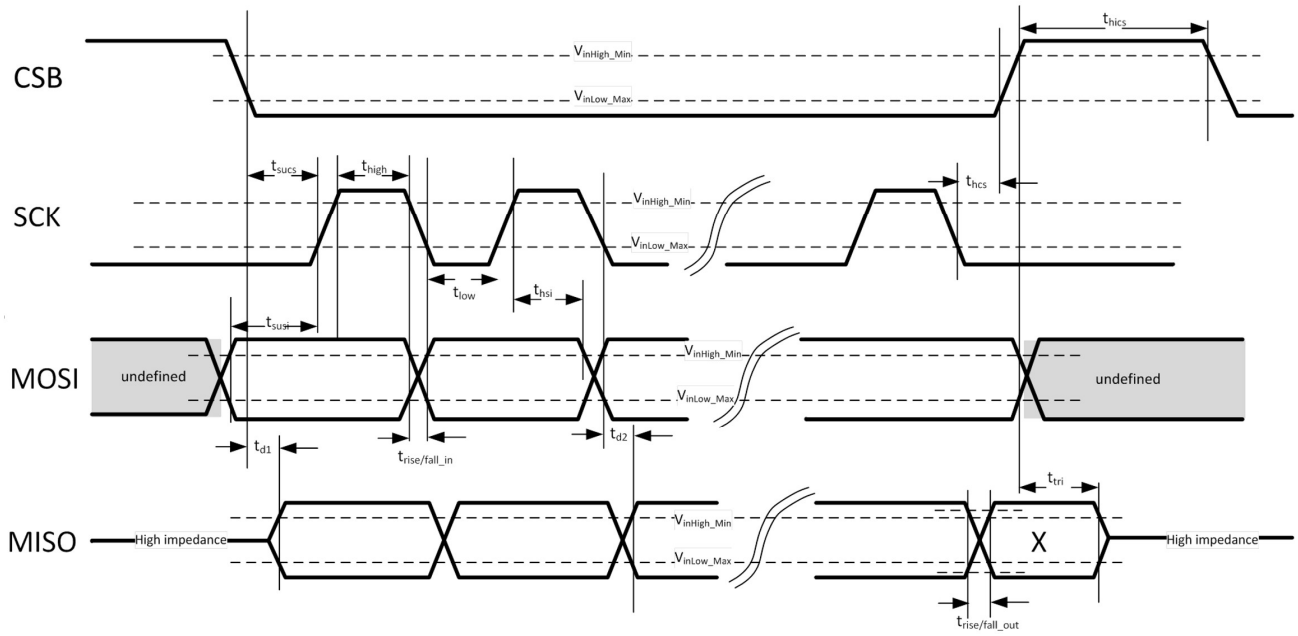


Figure 2. Timing diagram of SPI communication.

Table 13. SPI AC electrical characteristics.

Symbol	Description	Min.	Nom.	Max.	Unit
f_{SPI}	Master (MCU): SPI SCLK frequency	0.1	-	10	MHz
t_{SPI}	Master (MCU): SPI SCLK period	-	1/ f_{SPI}	-	-
t_{high}	Master (MCU): High time: duration of logical high level at SCLK (from V_{inHigh_min} to V_{inHigh_min})	35	$t_{SPI}/2$	-	ns
t_{low}	Master (MCU): Low time: duration of logical low level at SCLK (from V_{inLow_max} to V_{inLow_max})	35	$t_{SPI}/2$	-	ns
t_{sucs}	Master (MCU): Setup time CSB: time between the falling edge of CSB and the rising edge of SCLK (from V_{inLow_max} to V_{inLow_max})	40	$t_{SPI}/2$	-	ns
t_{susi}	Master (MCU): Setup time at MOSI: setup time of MOSI before the rising edge of SCLK (from V_{inLow_max} to V_{inLow_max} or from V_{inHigh_min} to V_{inLow_max})	10	-	-	ns
t_{hsi}	Master(MCU): Hold time at MOSI: hold time of MOSI after rising edge of SCLK (from V_{inHigh_min} to V_{inLow_max} or to V_{inHigh_min})	20	-	-	ns
t_{hcs}	Master (MCU): Hold time of CSB: time between the falling edge of SCLK and the rising edge of CSB (from V_{inLow_max} to V_{inLow_max})	30	$t_{SPI}/2$	-	ns

t_{hics}	Master (MCU): Minimum high time of CSB between two consecutive transfers (from V_{inHigh_min} to V_{inHigh_min})	30	$t_{SPI}/2$		ns
$t_{rise/fall\_in}$	Master (MCU): Rise/fall time of SCK/MOSI signals (from V_{inLow_max} to V_{inHigh_min} or from V_{inHigh_min} to V_{inLow_max})	-	-	0.15x t_{SPI}	ns
t_{d1}	Slave(=SCC400T ASIC): Delay time: time delay from the falling edge of CSB totab data valid at MISO (from V_{inLow_max} to V_{InLow_max} or to V_{InHigh_min})	-	-	30	ns
t_{d2}	Slave(=SCC400T ASIC): Delay time: time delay from falling edge of SCLK to data valid at MISO (from V_{inLow_max} to V_{InLow_max} or to V_{InHigh_min})	0	-	30	ns
t_{tri}	Slave(=SCC400T ASIC): Tri-state delay time: time between the rising edge of CSB to MISO in Tri-state (from V_{inHigh_min} to X)	-	-	25	ns
$t_{rise/fall\_out}$	Slave(=SCC400T ASIC): Rise/fall time of MISO signal ($V_{Out\_10\%}$ to $V_{Out\_90\%}$ and from $V_{Out\_90\%}$ to $V_{Out\_10\%}$) User selectable MISO slew rate control in Mode register (19h)	4	10	16	ns

2.13 Measurement Axis and Directions

Rx (1DOF) Rx-Rz-Ax-Ay-Az (5DOF)

Figure 3. SCC400T series measurement directions.

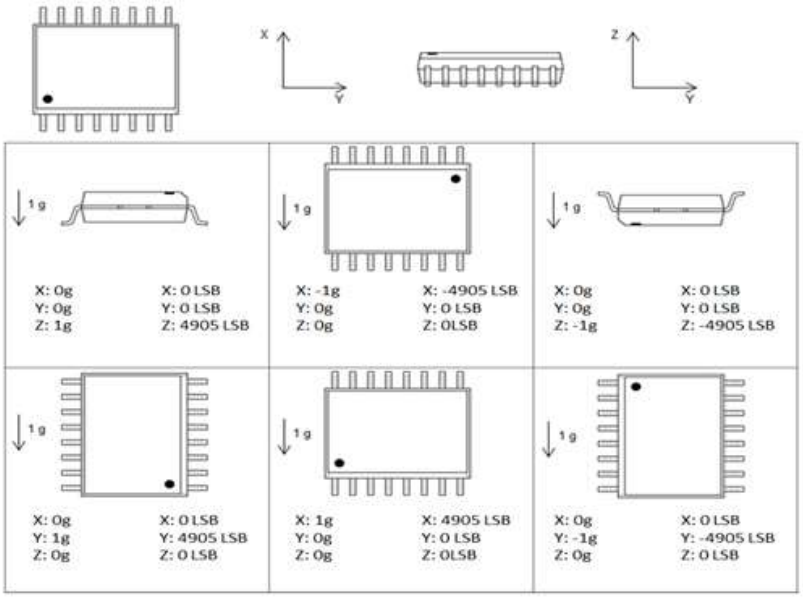


Figure 4 Accelerometer measurement directions and outputs (1g resolution depends on output channel).

2.14 Packing Characteristics

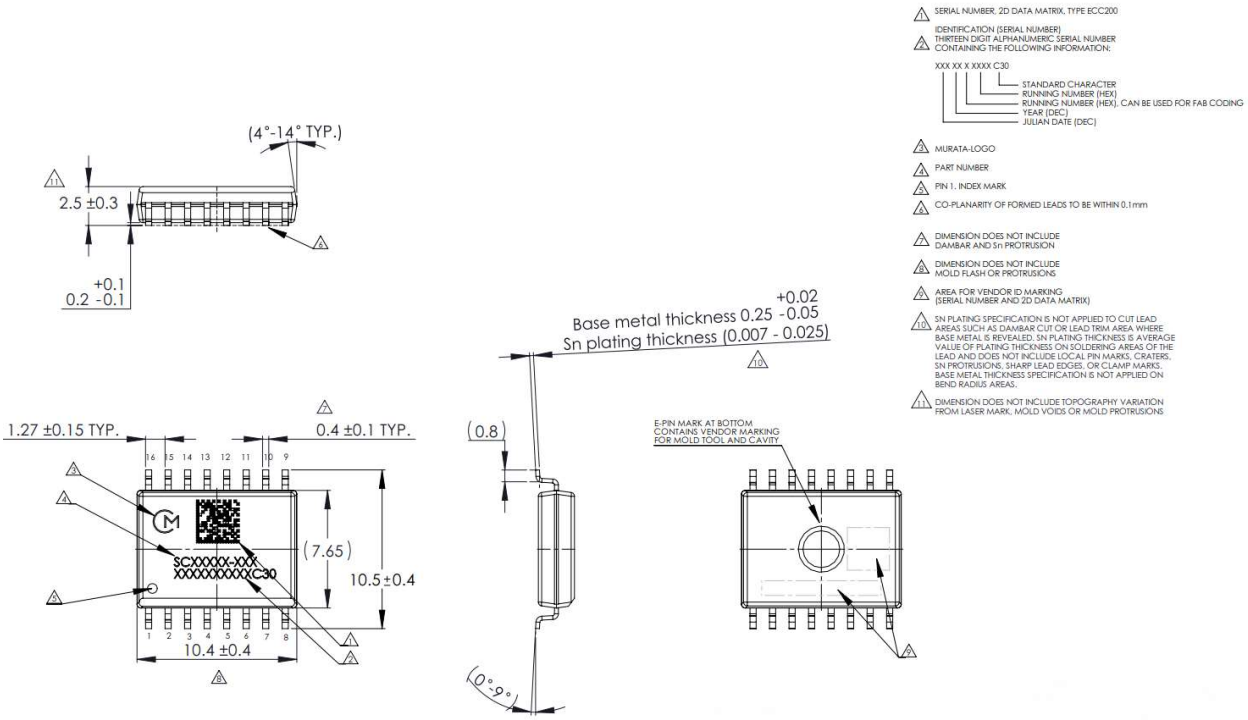


Figure 5. The outline of the SCC400T package (SOIC16-W) in mm.

2.15 PCB Footprint

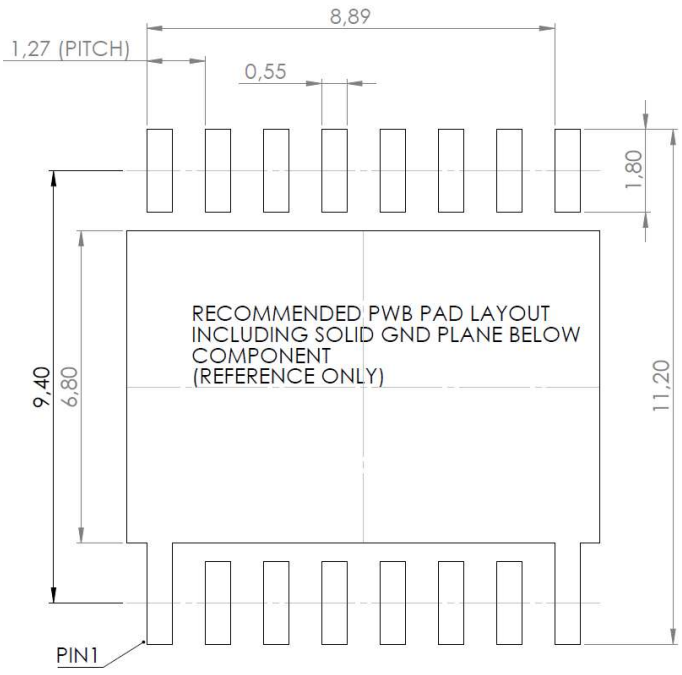


Figure 6. Recommended PWB pad layout for SCC400T.

For application schematic and PCB layout, please refer to chapter 9 Application information.

3 Assembly Instructions

The design of the application PCB, design of fixtures, conformal coating, vibration and mechanical shocks, material selections, application environment and component assembly process can have an impact on the sensor performance. Please refer to the document “APP 10207 Assembly instructions for SCC400T Series ENG” for related details.

4 Order codes

SCC433T-K03 order codes.

Order code	Description	Packing	Qty
SCC433T-K03-004	Combined gyro (X/Z-axis ±300°/s) and accelerometer (XYZ-axis ±6g & 8g) with SPI interface	bulk	4 pcs
SCC433T-K03-05		T&R	50 pcs
SCC433T-K03-10		T&R	1000 pcs

SCR410T-K03 order codes.

Order code	Description	Packing	Qty
SCR410T-K03-004	Gyro (X-axis ±300°/s) with SPI interface	bulk	4 pcs
SCR410T-K03-05		T&R	50 pcs
SCR410T-K03-10		T&R	1000 pcs

This is the end of publicly available document. For full version of this of this data sheet and assembly instructions, please contact Murata.

5 General Product Description

5.1 Component block diagram

SCC400T sensor consists of independent acceleration and angular rate sensing elements, and single Application-Specific Integrated Circuit (ASIC) used to sense and to control those elements. Figure 7 contains an upper level block diagram of the component. The ASIC provides one common SPI interface used to control and read the accelerometer and the gyroscope. SCC433T-K03 version has additional gyro block. ASIC supports parallel XYZ acceleration channels for LGS (Secondary accelerometer output) function to remove time uncertainty by compensating with 32×F_prim/2. For more details please see 7.1.7.

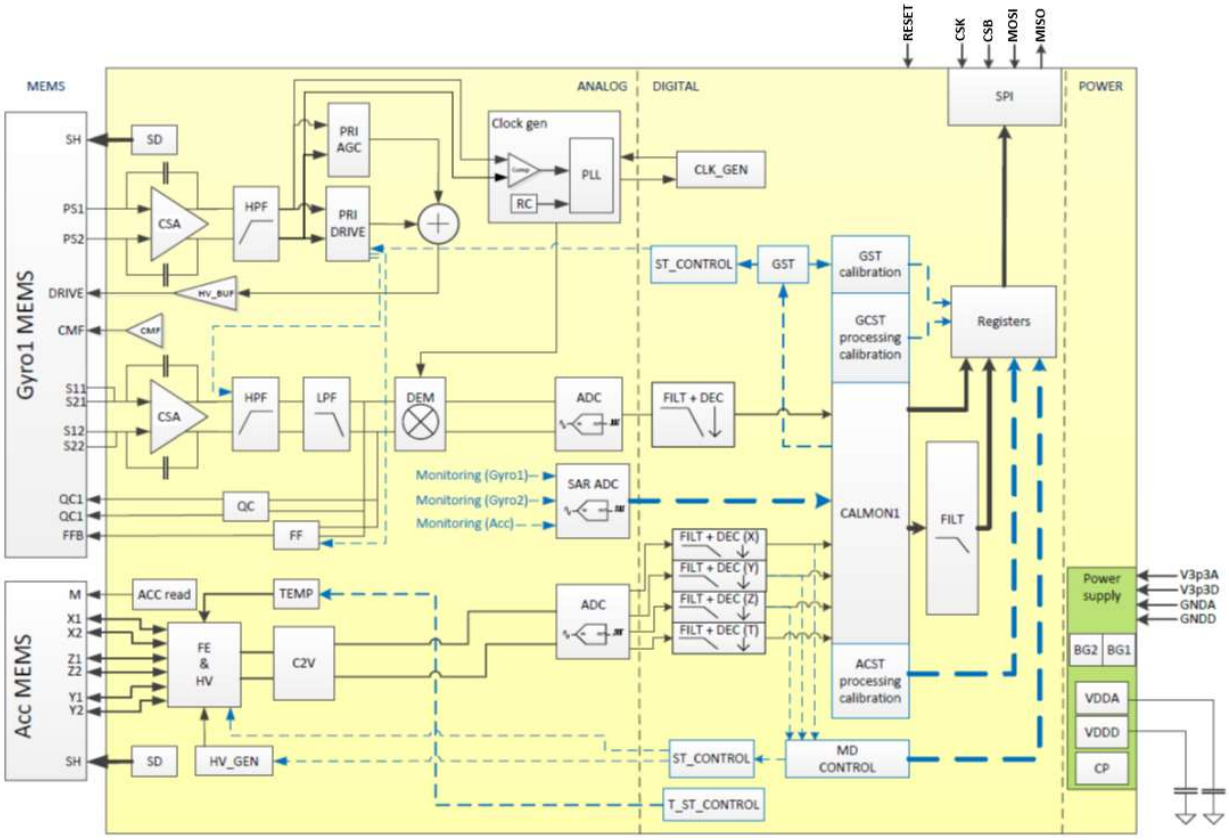


Figure 7. SCC400T component block diagram.

The angular rate and acceleration sensing elements are manufactured using Murata proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables making robust, extremely stable and low noise capacitive sensors.

5.2 Acceleration sensing element

The acceleration sensing element consists of three acceleration sensitive masses. Acceleration causes capacitance change that is converted into a voltage change in the signal conditioning ASIC.

5.3 Gyroscope sensing element

Z-Gyro sensing element consists of moving masses that are intentionally exited to in-plane drive motion. Rotation in sensitive direction causes in-plane movement that can be measured as capacitance change with the signal conditioning ASIC.

X-Gyro sensing element consists of moving masses that are purposely exited to in-plane drive motion. Rotation in sensitive direction causes out of plane movement that can be measured as capacitance change with the signal conditioning ASIC.

5.4 Factory Calibration

SCC400T sensors are factory calibrated. No separate calibration is required in the application. Parameters that are trimmed during production include offset and sensitivity for gyroscope and accelerometer. Fail safe monitoring signals are also calibrated. Offset and sensitivity are calibrated with 2nd order polynomial at -40°C, +25°C and +110°C. Calibration parameters are stored to non-volatile memory during manufacturing. The parameters are read automatically from the internal non-volatile memory during the start-up.

It should be noted that assembly can cause minor offset/bias errors to the sensor output. If best possible offset/bias accuracy is required, system level offset/bias calibration (zeroing) after assembly is recommended.

6 Component Operation, Reset and Power Up

6.1 Component Operation

SCC400T component has internal power-on reset circuit. It releases the internal reset-signal once the power supplies are within the specified range and reads configuration and calibration data from the non-volatile memory to volatile registers. After the memory read, the sensor goes to low power mode. An internal startup sequence is performed, when operation mode is activated by SPI command. 1DOF (SCR410T-K03) version requires 1 time of SPI write command and 5DOF (SCR433T-K03) version requires 2 times of SPI write command to set operation mode. Start-up time is dependent of low pass filter setting. After the power on or reset, sensor shall be able to provide valid acceleration and angular rate data after specified Power on Start-up time. SCC400T sensor uses lowest available low pass filter setting by default. In case some other low pass filter is desired the filter can be selected by SPI command. SCC400T component has extensive internal fail-safe diagnostics to detect over range and possible internal failures. The diagnostic status can be monitored via SPI RS - and status register bits.

6.2 Internal Failsafe Diagnostics

During the startup sequence the sensor performs a series of internal tests that will set various error flags in the sensor status registers and to clear them it is necessary to read summary status register after the startup sequence is complete.

Once startup sequence is completed and End of Initialization bit (EOI bit) has been written to one, the SPI frame Return Status bits (RS bits) indicate sensor operation status. Normal operation is indicated with RS bit content of 01b.

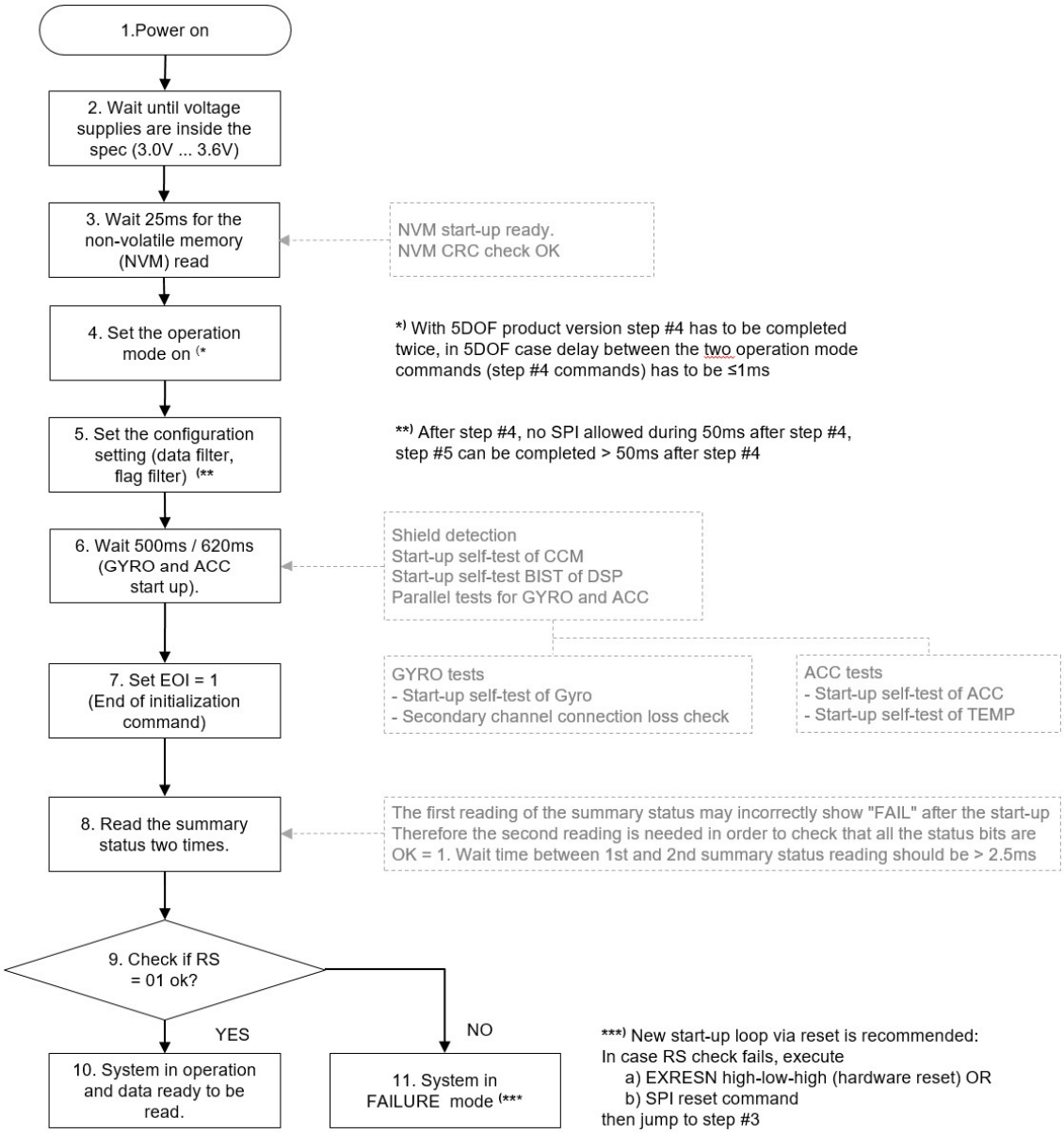


Figure 8. Power up sequence.

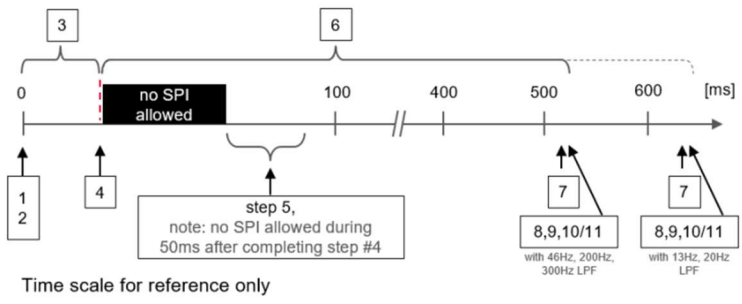


Figure 9. Timing diagram of the power up sequence (references to the steps in Figure 8).

7 Component Interfacing

7.1 SPI Interface

7.1.1 General

SCC400T has one common physical SPI interface for the accelerometer and the angular rate sensor. SPI communication transfers data between the SPI master and registers of SCC400T ASIC. SCC400T always operates as a slave device in master-slave operation mode. 3-wire SPI connection cannot be used.

SPI interface pins:

CSB	Chip Select (active low)	MCU → ASIC
SCK	Serial Clock	MCU → ASIC
MOSI	Master Out Slave In	MCU → ASIC
MISO	Master In Slave Out	ASIC → MCU

7.1.2 Protocol

SPI communication uses off-frame protocol so each transfer has two phases.

The first phase contains the SPI command (Request) and the data (Response) of the previous command. The second phase contains the next Request and the Response to the Request of the first phase, see Figure 10.

Data word length is 32 bits, the data is transferred MSB first. The first response after reset is undefined and shall be discarded.

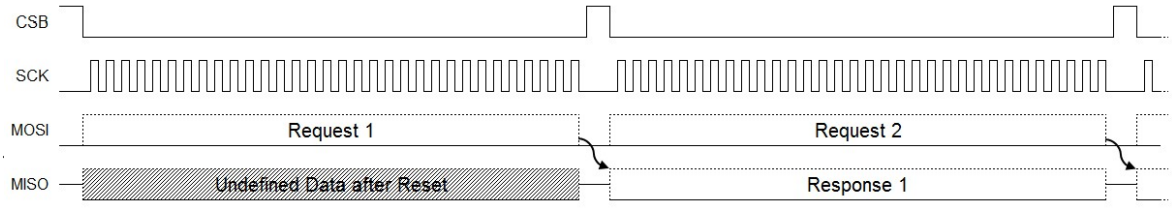


Figure 10. SPI protocol example.

The interleaved Request - Response cycle then continues as shown in Figure 11.

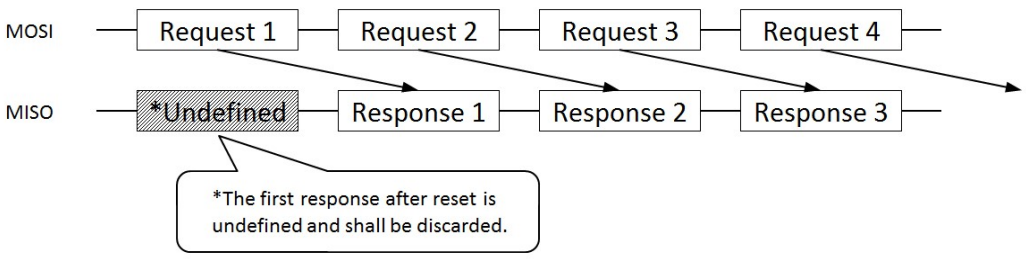


Figure 11. Request – Response frame relationship.

The SPI transmission is always started with the CSB falling edge and terminated with the CSB rising edge. The data is captured on the SCK's rising edge (MOSI line) and it is propagated on the SCK's falling edge (MISO line). This equals to SPI Mode 0 (CPOL = 0 and CPHA = 0), see Figure 12.

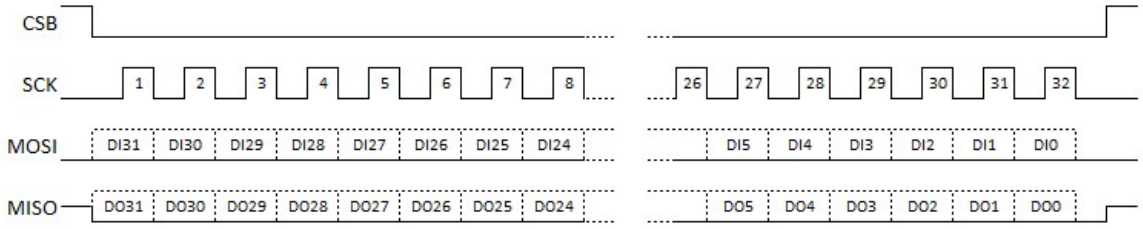


Figure 12. SPI Frame Format.

7.1.3 General Instruction format

The SPI frame is divided into four parts (See Figure 13 and Table):

1. Operation Code (OP)
2. Return status (RS, in MISO)
3. Data (DI, DO)
4. Checksum (CRC)

Unused bits shall be set to 0, this is important for the checksum calculation.

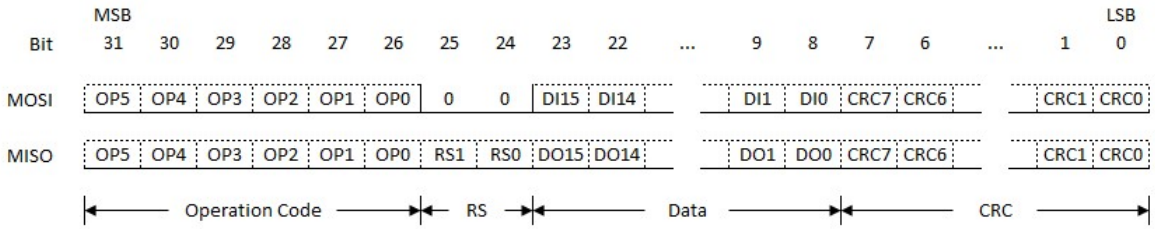


Figure 13. SPI instruction format.

Table 14. SPI bit definitions.

Bits	Name	MOSI	MISO
OP[5:0]	Operation code	Requested operation: • OP5: Write =1 / Read = 0 • OP[4:0] = Register address	Performed operation: • OP5: Write = 1 / Read = 0 • OP[4:0] = Register address
RS[1:0]	Return status	n.a.	Sensor status
D[15:0]	Data	Data to be written	Return data
CR[7:0]	Checksum	Checksum of MOSI bits [31:8]	Checksum of MISO bits [31:8]

7.1.4 Operations

Table 15. Operations and their equivalent SPI frames.

Operation	Register	SPI Frame Binary (OP, RS, Data, CRC)	SPI Frame Hex
Set Operation mode	MODE (19h)	111001 00 0000000000000000 01100111	E4000067h
Select 13Hz filter for RATE	G_FILT_DYN (16h)	110110 00 0000000000000000 01000101	D8000045h
Select 46Hz filter for RATE	G_FILT_DYN (16h)	110110 00 0001001000010010 10011110	D812129Eh
Select 13Hz filter for ACC	A_FILT_DYN (1Ah)	111010 00 0000000000000000 01101101	E800006Dh
Select 46Hz filter for RATE	A_FILT_DYN (1Ah)	111010 00 0000001000100010 01001000	E8022248h
Set EOI bit	ResCTRL (18h)	111000 00 0000000000000010 01011011	E000025Bh
Reset via SPI	ResCTRL (18h)	111000 00 0000000000000001 01111100	E000017Ch
Read RATE_X	RATE_X (01h)	000001 00 0000000000000000 11110111	040000F7h
Read RATE_Z	RATE_Z (03h)	000011 00 0000000000000000 11111011	0C0000FBh
Read ACC_X	ACCX (04h)	000100 00 0000000000000000 11101001	100000E9h
Read ACC_Y	ACCY (05h)	000101 00 0000000000000000 11101111	140000EFh
Read ACC_Z	ACCZ (06h)	000110 00 0000000000000000 11100101	180000E5h
Read TEMP	TEMP (07h)	000111 00 0000000000000000 11100011	1C0000E3h
Read AX_LGS	AX_LGS (08h)	001000 00 0000000000000000 11000001	200000C1h
Read AY_LGS	AY_LGS (09h)	001001 00 0000000000000000 11000111	240000C7h
Read AZ_LGS	AZ_LGS (0Ah)	001010 00 0000000000000000 11001101	280000CDh
Read RATE_X2	RATE_X2 (0Bh)	001011 00 0000000000000000 11001011	2C0000CBh
Read RATE_Z2	RATE_Z2 (0Dh)	001101 00 0000000000000000 11011111	340000DFh
Read Summary Status	S_Sum (0Eh)	001110 00 0000000000000000 11010101	380000D5h
Read Rate Status 1	R_S1 (10h)	010000 00 0000000000000000 10010001	40000091h
Read Rate Status 2	R_S2 (11h)	010001 00 0000000000000000 10010111	44000097h
Read Accelerometer Status	A_S1 (12h)	010010 00 0000000000000000 10011101	4800009Dh
Read Common Status 1	C_S1 (14h)	010100 00 0000000000000000 10001001	50000089h
Read Common Status 2	C_S2 (15h)	010101 00 0000000000000000 10001111	5400008Fh

ACC and ACC LGS is not functional for SCR410T-K03.

7.1.5 Return Status

SPI frame Return Status bits (RS bits) indicate the functional status of the sensor, see Return Status definitions in Table 16 and in Figure 14.

Table 16. Return Status definitions.

RS[1]	RS[0]	Description
0	0	Initialization running
0	1	Normal operation of selected channel
1	0	Selftest of selected channel ongoing or not started
1	1	Reserved or not existing register addressed, error of selected channel or common failure

The priority of the return status states is from high to low: 10 → 00 → 11 → 01.

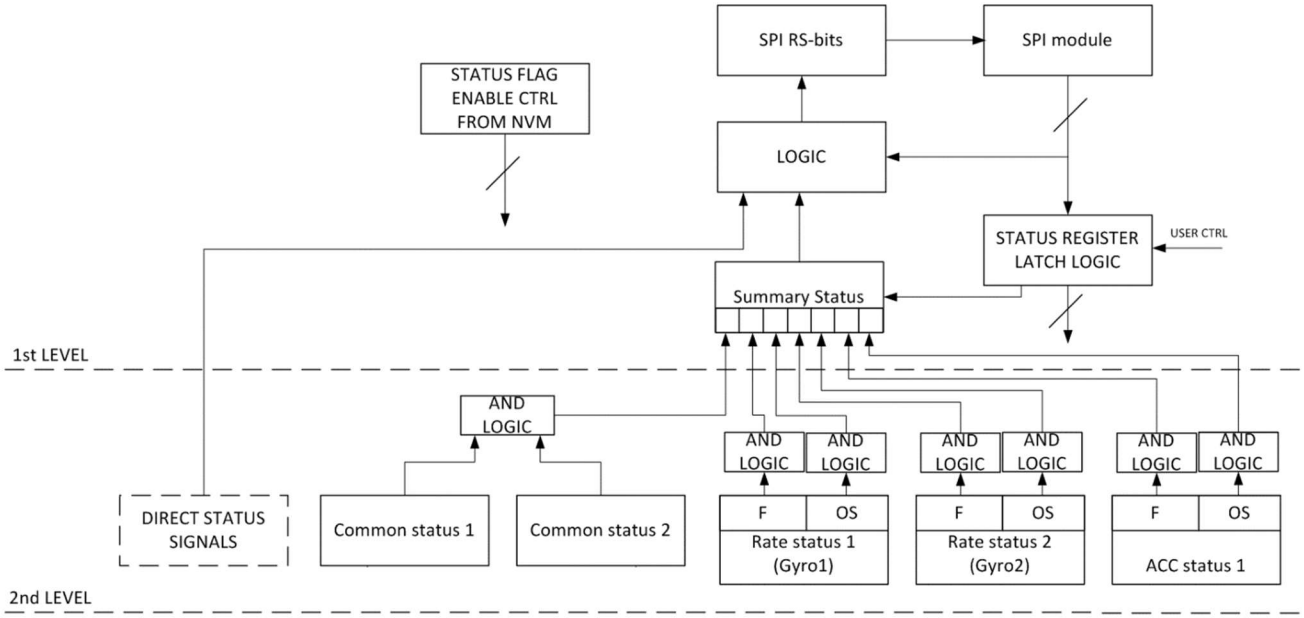


Figure 14. Return Status (RS) bits (in the 1st level) will be generated via logic from various sources in the 2nd level.

7.1.6 Checksum (CRC)

For SPI transmission error detection a Cyclic Redundancy Check (CRC) is implemented, for details see Table 17.

Table 17. SPI CRC definition.

Parameter	Value
Name	CRC-8
Width	8 bit
Poly	1Dh (generator polynom: X8+X4+X3+X2+1)
Init	FFh (initialization value)
XOR out	FFh (inversion of CRC result)

The CRC value used in system level software has to be initialized with FFh to ensure a CRC failure in case of stuck-at-0 and stuck-at-1 error on the SPI bus. C-programming language example for CRC calculation is presented in Figure 15. It can be used as is in an appropriate programming context.

```
// Calculate CRC for 24 MSB's of the 32 bit dword
// (8 LSB's are the CRC field and are not included in CRC calculation)
uint8_t CalculateCRC(uint32_t Data)
{
  uint8_t BitIndex;
  uint8_t BitValue;
  uint8_t CRC;

  CRC = 0xFF;
  for (BitIndex = 31; BitIndex > 7; BitIndex--)
  {
    BitValue = (uint8_t)((Data >> BitIndex) & 0x01);
    CRC = CRC8(BitValue, CRC);
  }
  CRC = (uint8_t)~CRC;
  return CRC;
}

static uint8_t CRC8(uint8_t BitValue, uint8_t CRC)
{
  uint8_t Temp;

  Temp = (uint8_t)(CRC & 0x80);
  if (BitValue == 0x01)
  {
    Temp ^= 0x80;
  }
  CRC <<= 1;
  if (Temp > 0)
  {
    CRC ^= 0x1D;
  }
  return CRC;
}
```

Figure 15. C-programming language example for CRC calculation.

CRC calculation example:
Read RATE register (01h) -> SPI[31:8] = 040000h -> CRC [7:0] -> F7h.
Further examples can be found in Table 15.

7.1.7 Output data rate

Accelerometer, Gyro and temperature data outputs have output data rate of F_prim/2.

The output data rate of secondary ACC (LGS) channels is 16×F_prim. The purpose of LGS interpolation is to remove time uncertainty by compensating with 32×F_prim/2. But it is one cycle late signal. ACC LGS is not available for SCR410T-K03.

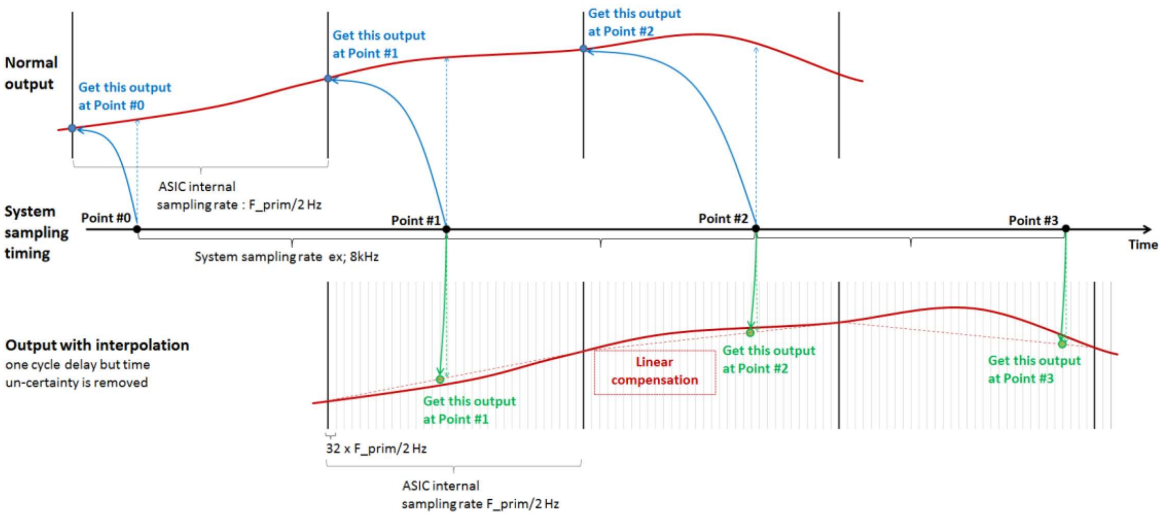


Figure 16. Secondary accelerometer (LGS) channels interpolation

8 Register Definition

Table 18. Address space overview.

Reg (hex)	R/W	Register Name	Description
00h	N/A	Reserved	Reserved
01h	R	RATE_X	X angular rate output
02h	N/A	Reserved	Reserved
03h	R	RATE_Z	Z angular rate output
04h	R	ACC_X	X acceleration channels output
05h	R	ACC_Y	Y acceleration channels output
06h	R	ACC_Z	Z acceleration channels output
07h	R	TEMP	Temperature sensor output
08h	R	AX_LGS	Parallel X acceleration output for Secondary accelerometer output
09h	R	AY_LGS	Parallel Y acceleration output for Secondary accelerometer output
0Ah	R	AZ_LGS	Parallel Z acceleration output for Secondary accelerometer output
0Bh	R	RATE_X2	Parallel X angular rate output
0Ch	N/A	Reserved	Reserved
0Dh	R	RATE_Z2	Parallel Z angular rate output
0Eh	R	S_Sum	Status summary
0Fh	R/W	SCtrl	Safe Control
10h	R	R_S1	Rate Status 1 (X angular rate status)
11h	R	R_S2	Rate Status 2 (Z angular rate status)
12h	R	A_S1	Accelerometer Status
13h	N/A	Reserved	Reserved
14h	R	C_S1	Common Status 1
15h	R	C_S2	Common Status 2
16h	R/W	G_FILT_DYN	Gyro filter control
17h	R/W	SYS_TEST	Test
18h	R/W	ResCTRL	Reset Control
19h	R/W	Mode	Mode
1Ah	R/W	A_FILT_DYN	Accelerometer filter control
1Bh	R	C_ID	Component ID 1
1Ch	R	T_ID2	Traceability 2
1Dh	R	T_ID0	Traceability 0
1Eh	R	T_ID1	Traceability 1

R/W operation to Reserved registers sets RS bits to ‘11’. User should not access to Reserved registers. Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.1 Sensor Data Block

Table 19. Sensor data block

Addr OP[4:0]	Bits	Register Name	No. of Bits	Read/ Write	Description
01h	[15:0]	RATE_X	16	R	Rate output in 2's complement format
03h	[15:0]	RATE_Z	16	R	Rate output in 2's complement format
04h	[15:0]	ACC_X	16	R	X-axis 6g acceleration output in 2's complement format
05h	[15:0]	ACC_Y	16	R	Y-axis 6g acceleration output in 2's complement format
06h	[15:0]	ACC_Z	16	R	Z-axis 6g acceleration output in 2's complement format
07h	[15:0]	TEMP	16	R	Temperature sensor output in 2's complement format.
08h	[15:0]	AX_LGS	16	R	Secondary X-axis 8g acceleration output in 2's complement format
09h	[15:0]	AY_LGS	16	R	Secondary Y-axis 8g acceleration output in 2's complement format
0Ah	[15:0]	AZ_LGS	16	R	Secondary Z-axis 8g acceleration output in 2's complement format
0Bh	[15:0]	RATE_X2	16	R	Parallel X angular rate output in 2's complement format
0Dh	[15:0]	RATE_Z2	16	R	Parallel Z angular rate output in 2's complement format

SPI read frames with CRC content for these registers are shown in Table 15. Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.1.1 Example of Angular Rate Data Conversion

For example, if RATE X register (01h) read results: RATE X = **05FFE08B**h, the register content is converted to angular rate as follows:

- 05h = 000001 01b
  - 000001b = operation code = Read RATE X
  - 01b = return status (RS bits) = no error
- FFE0h = 1111 1111 1110 0000b = RATE X register content
  - FFE0h in 2's complement format = -32d
  - Angular rate = -32LSB / sensitivity = -32LSB / (80LSB/(°/s)) = -0.4°/s
- 8Bh = CRC of 05FFE0h

8.1.2 Example of Acceleration Data Conversion

For example, if ACC_X register read results: ACC_X = **1100DC02**h, the register content is converted to acceleration rate as follows:

- 11h = 000100 01b
  - 000100b = operation code = Read ACC_X
  - 01b = return status (RS bits) = no error
- 00DCh = bin 0000 0000 1101 1100b = ACC_X register content
  - 00DCh in 2's complement format = 220d
  - Acceleration = 220LSB / sensitivity = 220LSB / (4905LSB/g) = 0.045g
- 02h = CRC of 1100DCh

Sensitivity is different for secondary accelerometer output LGS signal (AX_LGS, AY_LGS, AZ_LGS).

8.1.3 Example of Temperature Data Conversion

For example, if TEMP register read results: TEMP = **1DFE6F4E**h, the register content is converted to temperature as follows:

- 1Dh = bin 000111 01b
  - bin 000111b = operation code = Read TEMP
  - 01 = return status (RS bits) = no error
- FE6Fh = bin 1111 1110 0110 1111 = TEMP register content
  - FE6Fh in 2's complement format = -401d
  - Temperature = 25 + (TEMP / 30) = 25 + [-401/30] = +11.6°C
  - See section 2.8 for temperature conversion equation
- 4Eh = CRC of 1DFE6Fh

8.2 Sensor Status Block and Control

Table 20. Sensor status block and control.

Addr OP[4:0]	Bits	Register Name	No. of Bits	Read/ Write	Description
0Eh	[15:0]	S_Sum	16	R	Summary Status
0Fh	[15:0]	SCtrl	16	R/W	Safe control
10h	[15:0]	R_S1	16	R	Rate_X Status (X-Gyro status)
11h	[15:0]	R_S2	16	R	Rate_Z Status (Z-Gyro status)
12h	[15:0]	A_S1	16	R	Accelerometer Status 1
14h	[15:0]	C_S1	16	R	Common Status 1
15h	[15:0]	C_S2	16	R	Common Status 2
16h	[15:0]	G_FILT_DYN	16	R/W	Gyro filter and dynamic control
17h	[15:0]	SYS_TEST	16	R/W	Dummy R/W register for system R/W tests. Not locked by EOI bit
18h	[15:0]	ResCtrl	16	R/W	Reset Control, ACC Z-channel saturation level and EOI set
19h	[15:0]	Mode	16	R/W	Mode Register
1Ah	[15:0]	A_FILT_DYN	16	R/W	ACC filter and dynamic control

R/W for the register means, that the content of the register can be read, and that it is also possible to overwrite the content of the register in normal mode operation if EOI is 0. If EOI=1 only the reset bit b0 of ResCtrl register and SYS_TEST register can be written. The following signal blocks will then operate with the value written to the register. After a write cycle to the register, the register will keep its value until another write cycle or reset occurs.

SPI read and write frames with CRC content for these registers are shown in Table 15.

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.1 Summary Status Register, S_Sum (0Eh)

Table 21. Summary Status register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
S_OK_C	S_OK_Rz_F	S_OK_Rz_OS	S_OK_Rx_F	S_OK_Rx_OS	S_OK_Ax_F	S_OK_Ax_OS	S_OK_LGSx_OS	S_OK_Ay_F	S_OK_Ay_OS	S_OK_LGSy_OS	S_OK_Az_F	S_OK_Az_OS	S_OK_LGSz_OS	STUP_OK_GX	STUP_OK_GZ	Read

Summary Status register indicates saturation or failure in component. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 22. Summary Status register bit description.

Register bit	Description
S_OK_C	Status summary flag for **common** blocks (1 = OK)
S_OK_Rz_F	Status summary flag for **RATE Z**-AXIS (expect *OS) (1 = OK) * Constant 0 for the product type without Z-Gyro
S_OK_Rz_OS	Status summary of saturation flags for **RATE Z**-AXIS (1 = OK) * Constant 0 for the product type without Z-Gyro
S_OK_Rx_F	Status summary flag for **RATE X**-AXIS (expect *OS) (1 = OK) * Constant 0 for the product type without X-Gyro
S_OK_Rx_OS	Status summary of saturation flags for **RATE X**-AXIS (1 = OK) * Constant 0 for the product type without X-Gyro
S_OK_Ax_F	Status summary flag for **ACC X**-AXIS (expect *OS) (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
S_OK_Ax_OS	Status summary of saturation flags for **ACC X**-AXIS (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
S_OK_LGSx_OS	Status summary of saturation flags for **ACC LGS X**-AXIS (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
S_OK_Ay_F	Status summary flag for **ACC Y**-AXIS (expect *OS) (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
S_OK_Ay_OS	Status summary of saturation flags for **ACC Y**-AXIS (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
S_OK_LGSy_OS	Status summary of saturation flags for **ACC LGS Y**-AXIS (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
S_OK_Az_F	Status summary flag for **ACC Z**-AXIS (expect *OS) (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
S_OK_Az_OS	Status summary of saturation flags for **ACC Z**-AXIS (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
S_OK_LGSz_OS	Status summary of saturation flags for **ACC LGS Z**-AXIS (1 = OK) * Constant 0 for the product type without accelerometer (Gyro only version)
STUP_OK_GX	Status summary flag of **startup** functions (1 = OK) * Constant 1 for the product type without X-Gyro
STUP_OK_GZ	Status summary flag of **startup** functions (1 = OK) * Constant 1 for the product type without Z-Gyro

OS: Output saturation condition

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.2 Safe Control Register, SCtrl (0Fh)

Table 23. Safe Control register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Write
Gsat[3:0]				Asat[3:0]				Stat_rmode	St_req_ccm	St_req_temp	St_req_ZGyro	St_req_XGyro	St_req_ACC	St_req_sys	Sat_mode	Read

Table 24. Safe Control register bit description.

Register bit	Description
Gsat[3:0]	Saturation flag filtering of rate signals. User can set the counter value, which is used to filter short output saturation periods before post filter. Same control is used for all rate outputs. Time is between Gsat x LSB and (Gsat+1) x LSB. One counter LSB=32 x F_pri_period
Asat[3:0]	Saturation flag filtering of acceleration signals including LGS. User can set the counter value, which is used to filter short output saturation periods before post filter. Same control is used for all acceleration outputs. Time is between Asat x LSB and (Asat+1) x LSB. One counter LSB=32 x F_pri_period
Stat_rmode	Status read mode 0 - Reading of Summary Status register "S_Sum" will clear all Bank0 status registers to 1 after delay of 36 x F_prim_period 1 - Reading of Summary Status register "S_Sum" will clear all Bank0 status registers to 1 without delay Note1: After reading of “S_Sum”, the delay of ≥2.5ms is required before “Stat_rmode” can be written 1 Note2: Reading other status register than S_Sum will clear the read status register to 1 without delay regardless of Stat_rmode value. Note3: 36 x F_prim_period depends on product type. 1DOF (X-Gyro version) : 2.02-2.28ms 5DOF (XZ-Gyro version) : 2.02-2.28ms
St_req_ccm	Request CCM self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
St_req_temp	Request Temperature start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
St_req_ZGyro	Request Z-Gyro start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
St_req_XGyro	Request X-Gyro start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
St_req_ACC	Request ACC channels start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
St_req_sys	Request system start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.

Sat_mode	Saturation flag mode selection, common for all output data saturation flags: 0 - (default) Error flag is set when saturation occurs and it has to be acknowledged (SPI read) by user before setting saturation status to OK state. 1 - Error flag is set when saturation occurs and it is automatically removed when saturation does not occur anymore. This setting shall not be used (refer the note). Note: When sat_mode=1 is used in addition to OS flags, A_S1 CST and other flags below are handled like OS flags and cleared automatically after failure. However, S_Sum is not cleared without read. CST_X_OK CST_Y_OK CST_Z_OK ACC_PP_CRC_OK STU_MD_STAT_OK

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.3 Rate Status 1 Register, R_S1 (10h)

Rate Status 1 register shows X-Gyro status

Table 25. Rate Status 1 register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
OVS_ANA1_OK	OVS_DIG1_OK	CST_G1_OK	GST_G1_OK	PLL_OSC_FG1_OK	MON_VCMF_G1_OK	MON_PRI1_FE_OK	MON_SEC1_FE_OK	MON_DRV_G1_OK	MON_AGC_G1_OK	MON_QC_G1_OK	MON_LPF_G1_OK	Reserved	MEMS_INT_G1_OK	GX_PP_CRC_OK	G1_PRI_OK	Read

Table 26. Rate Status 1 register bit description.

Register bit	Description
OVS_ANA1_OK	Overflow Saturation status of X-Gyro analog part (1 = OK)
OVS_DIG1_OK	Overflow Saturation status of X-Gyro digital part (1 = OK)
CST_G1_OK	X-Gyro Continuous self-test ok (1 = OK)
GST_G1_OK	X-Gyro Start-up self-test ok (1 = OK)
PLL_OSC_FG1_OK	X-Gyro PLL frequency comparison to RC oscillator (1 = OK)
MON_VCMF_G1_OK	X-Gyro CCM Monitoring: VCMF1 ok (1 = OK)
MON_PRI1_FE_OK	X-Gyro primary front end ok (1 = OK)
MON_SEC1_FE_OK	X-Gyro secondary front end ok (1 = OK)
MON_DRV_G1_OK	CCM Monitoring: X-Gyro drive path ok (1 = OK)
MON_AGC_G1_OK	CCM Monitoring: X-Gyro AGC ok (1 = OK)
MON_QC_G1_OK	CCM Monitoring: X-Gyro quadrature compensation path ok (1 = OK)
MON_LPF_G1_OK	CCM Monitoring: X-Gyro force-feedback path ok (1 = OK)
Reserved	Bit value fixed to 1
MEMS_INT_G1_OK	X-Gyro MEMS interface ok (1 = OK)
GX_PP_CRC_OK	X-Gyro filter coefficient CRC status (1 = OK)
G1_PRI_OK	X-Gyro primary channel ok (1 = OK)

8.2.4 Rate Status 2 Register, R_S2 (11h)

Rate Status 2 register shows Z-Gyro status

Table 27. Rate Status 2 register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
OVS_ANA2_OK	OVS_DIG2_OK	CST_G2_OK	GST_G2_OK	PLL_OSC_FG2_OK	MON_VCMF_G2_OK	MON_PRI2_FE_OK	MON_SEC2_FE_OK	MON_DRV_G2_OK	MON_AGC_G2_OK	MON_QC_G2_OK	MON_LPF_G2_OK	Reserved	MEMS_INT_G2_OK	DSP2_OK (5DOF)	G2_PRI_OK	Read

Table 28. Rate Status 2 register bit description.

Register bit	Description
OVS_ANA2_OK	Overflow Saturation status of Z-Gyro analog part (1 = OK)
OVS_DIG2_OK	Overflow Saturation status of Z-Gyro digital part (1 = OK)
CST_G2_OK	Z-Gyro Continuous self-test ok (1 = OK)
GST_G2_OK	Z-Gyro Start-up self-test ok (1 = OK)
PLL_OSC_FG2_OK	Z-Gyro PLL frequency comparison to RC oscillator (1 = OK)
MON_VCMF_G2_OK	Z-Gyro CCM Monitoring: VCMF2 ok (1 = OK)
MON_PRI2_FE_OK	Z-Gyro primary front end ok (1 = OK)
MON_SEC2_FE_OK	Z-Gyro secondary front end ok (1 = OK)
MON_DRV_G2_OK	CCM Monitoring: Z-Gyro drive path ok (1 = OK)
MON_AGC_G2_OK	CCM Monitoring: Z-Gyro AGC ok (1 = OK)
MON_QC_G2_OK	CCM Monitoring: Z-Gyro quadrature compensation path ok (1 = OK)
MON_LPF_G2_OK	CCM Monitoring: Z-Gyro force-feedback path ok (1 = OK)
Reserved	Bit value fixed to 1
MEMS_INT_G2_OK	Z-Gyro MEMS interface ok (1 = OK)
DSP2_OK (5DOF)	Digital signal processor2 and Z-Gyro filter coefficient CRC status OK (1 = OK) (DSP1 (X-Gyro) status is found from common status 2 register)
G2_PRI_OK	Z-Gyro primary channel ok (1 = OK)

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.5 Accelerometer Status 1 Register, A_S1 (12h)

Table 29. Accelerometer Status 1 register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
OVS_ANA_ACCX_OK	OVS_ANA_ACCY_OK	OVS_ANA_ACCZ_OK	OVS_DIG_ACCX_OK	OVS_DIG_ACCY_OK	OVS_DIG_ACCZ_OK	OVS_DIG_LGSX_OK	OVS_DIG_LGSY_OK	OVS_DIG_LGSZ_OK	CST_X_OK	CST_Y_OK	CST_Z_OK	ACC_PP_CRC_OK	STU_MD_STAT_OK	STAT_SD_ACC_OK	Reserved	Read

Table 30. Accelerometer Status register bit description.

Register bit	Description
OVS_ANA_ACCX_OK	Overflow Saturation status of ACCX analog part (1 = OK)
OVS_ANA_ACCY_OK	Overflow Saturation status of ACCY analog part (1 = OK)
OVS_ANA_ACCZ_OK	Overflow Saturation status of ACCZ analog part (1 = OK)
OVS_DIG_ACCX_OK	Overflow Saturation status of ACCX digital part (1 = OK)
OVS_DIG_ACCY_OK	Overflow Saturation status of ACCY digital part (1 = OK)
OVS_DIG_ACCZ_OK	Overflow Saturation status of ACCZ digital part (1 = OK)
OVS_DIG_LGSX_OK	Overflow Saturation status of LGSX digital part (1 = OK)
OVS_DIG_LGSY_OK	Overflow Saturation status of LGSY digital part (1 = OK)
OVS_DIG_LGSZ_OK	Overflow Saturation status of LGSZ digital part (1 = OK)
CST_X_OK	Status of continuous self-test of ACCX and LGSX (1=OK)
CST_Y_OK	Status of continuous self-test of ACCY and LGSY (1=OK)
CST_Z_OK	Status of continuous self-test of ACCZ and LGSZ (1=OK)
ACC_PP_CRC_OK	ACC filter coefficient CRC status (1=OK)
STU_MD_STAT_OK	Status of ACC start-up mass deflection self-test (1=OK)
STAT_SD_ACC_OK	Status of ACC shield detection self-test (1=OK)

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.6 Common Status 1 Register, C_S1 (14h)

Table 31. Common Status 1 register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
EOI_state	STDIS_C	STDIS_Rz	STDIS_Rx	STDIS_A	BIST_DSP2_DONE	MCLK2_stat (5DOF)	Reserved	Reserved	Reserved	Nmode_OK	NVM_START_OK	HV_OK	CRC_SPI_OK	CRC_REG_OK	CRC_NVM_OK	Read

Table 32. Common Status 1 register bit description.

Register bit	Description
EOI_state	End of Initialization: Start-up sequence completed ok (1 = OK)
STDIS_C	All common start-up self-tests inactive/active (1 = inactive / 0 = active)
STDIS_Rz	Status of all the Z-Gyro start-up self-tests: currently inactive/active (1 = inactive / 0 = active)
STDIS_Rx	Status of all the X-Gyro start-up self-tests: currently inactive/active (1 = inactive / 0 = active)
STDIS_A	All ACC start-up self-tests disabled/enabled (1 = disabled / 0 = enabled)
BIST_DSP2_DONE	Built-in self-test of Digital signal processor2 done, valid only for 5DOF version. Constant 1 for other versions In 1DOF X-Gyro version, DSP1 is X-Gyro (No DSP2) In 5DOF XZ-Gyro version, DSP1 is X-Gyro and DSP2 is Z-Gyro
MCLK2_stat (5DOF)	Comparison of PLL signals from gyro 1 and gyro 2
Nmode_OK	Normal mode OK (1 = normal mode; 0 = any test mode activated)
NVM_START_OK	NVM module OK (1 = OK)
HV_OK	HV generator OK (1 = OK)
CRC_SPI_OK	SPI CRC comparison OK (1 = OK)
CRC_REG_OK	Register map CRC OK (1 = OK)
CRC_NVM_OK	NVM CRC OK (1 = OK)

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.7 Common Status 2 Register, C_S2 (15h)

Table 33. Common Status 2 register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
MON_TEMP_OK	MON_FAIL_P_OK	MON_V3p3D_OK	MON_V3p3A_OK	MON_DVBG_OK	MON_FAIL_N_OK	MON_VDDD_OK	TEMP_ANA_OK	CCM_CAL_OK	Reserved	Reserved	Reserved	TEMP_CALC_OK	DSP1_CLOCK_OK	DSP1_OK	ST_STAT_TEMP	Read

Table 34. Common Status 2 register bit description.

Register bit	Description
MON_TEMP_OK	CCM Monitoring: Temperature sensor OK (1 = OK)
MON_FAIL_P_OK	CCM Monitoring: FAIL_P OK (1 = OK)
MON_V3p3D_OK	CCM Monitoring: V3p3D voltage supply OK (1 = OK)
MON_V3p3A_OK	CCM Monitoring: V3p3A voltage supply OK (1 = OK)
MON_DVBG_OK	CCM Monitoring: DVBG OK (1 = OK)
MON_FAIL_N_OK	CCM Monitoring: FAIL_N OK (1 = OK)
MON_VDDD_OK	CCM Monitoring: VDDD OK (1 = OK)
TEMP_ANA_OK	Temperature analog data path ok (1 = OK)
CCM_CAL_OK	CCM internal monitoring OK (1 = OK)
TEMP_CALC_OK	Ok status of temperature calculations (1=OK)
DSP1_CLOCK_OK	Digital signal processor1 clock OK (1 = OK) In 1DOF X-Gyro version, DSP1 is X-Gyro (No DSP2) In 5DOF XZ-Gyro version, DSP1 is X-Gyro and DSP2 is Z-Gyro
DSP1_OK	Digital signal processor1 OK (1 = OK) In 1DOF X-Gyro version, DSP1 is X-Gyro (No DSP2) In 5DOF XZ-Gyro version, DSP1 is X-Gyro and DSP2 is Z-Gyro (See Rate Status 2 Register)
ST_STAT_TEMP	Status of Temperature start-up self-test (1=OK)

8.2.8 Gyro filter control, G_FILT_DYN (16h)

Table 35. Gyro filter and dynamic control register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Write
Reserved	RX2_DYN	RX2_FILT[2]	RX2_FILT[1]	RX2_FILT[0]	RX_FILT[2]	RX_FILT[1]	RX_FILT[0]	Reserved	RZ2_DYN	RZ2_FILT[2]	RZ2_FILT[1]	RZ2_FILT[0]	RZ_FILT[2]	RZ_FILT[1]	RZ_FILT[0]	Read

Table 36. Gyro filter and dynamic control register bit description.

Register bit	Description
RX2_DYN	RX2 output dynamic range selection 0 - nominal dynamic range 1 - nominal dynamic range divided by 2 It's shift option after post filter (only digital gain). LSB step is half and quantization noise is half.
RX2_FILT[2] RX2_FILT[1] RX2_FILT[0]	RX2 filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter (not recommended, see gyro noise specifications with and without CST) 1xx - 300Hz 3rd order filter
RX_FILT[2] RX_FILT[1] RX_FILT[0]	RX filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter (not recommended, see gyro noise specifications with and without CST) 1xx - 300Hz 3rd order filter
RZ2_DYN	RZ2 output dynamic range selection 0 - nominal dynamic range 1 - nominal dynamic range divided by 2 It's shift option after post filter (only digital gain). LSB step is half and quantization noise is half.
RZ2_FILT[2] RZ2_FILT[1] RZ2_FILT[0]	RZ2 filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter (not recommended, see gyro noise specifications with and without CST) 1xx - 300Hz 3rd order filter
RZ_FILT[2] RZ_FILT[1] RZ_FILT[0]	RZ filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter (not recommended, see gyro noise specifications with and without CST) 1xx - 300Hz 3rd order filter

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.9 Test register, SYS_TEST (17h)

16bit read/write register which can be used to check the accessibility of the device or if multiple devices are connected to the SPI bus, to check if the SC signals are working properly. 17h register is not locked by EOI bit.

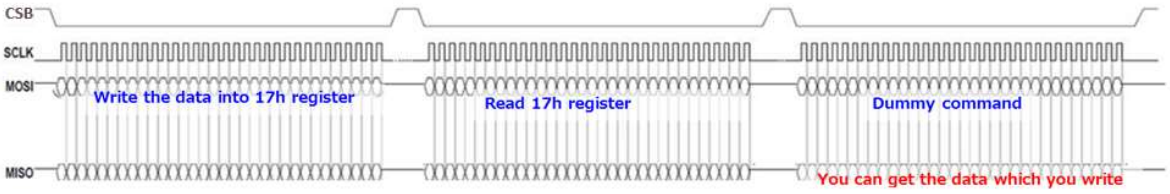


Figure 17. Test register operation

8.2.10 Reset Control Register, ResCTRL (18h)

Table 37. Reset Control register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	Yes	Yes	Yes	Yes	Yes	Yes	Write
Reserved										TDEL_CTRL[1]	TDEL_CTRL[0]	Reserved		EOI	HardReset	Read

Table 38. Reset control register bit description.

Register bit	Description
TDEL_CTRL[1]	S_Sum TDEL (if Stat_rmode=0 in 0F'h register): 00 - 36864 x MCLK [1.7...2.4ms] 01 - 15360 x MCLK [0.7...1.0ms] 10 - 7680 x MCLK [0.3...0.5ms] 11 - 1920 x MCLK [0.089...0.123ms] Note: TDEL is started by read of S_Sum. If detailed status registers are read after S_Sum read, they need to be read during TDEL time, otherwise the failure information is lost.
TDEL_CTRL[0]	
EOI	**End of Initialization**, lock all R/W registers (expect Hardreset bit in this register) and SYS_TEST register, reset needed to set EOI=0 This bit can be set/written to '1' only if all start-up self-tests have been completed. 1 - Normal operation 0 - Initiliazation state, SPI RS cannot be 01 (normal operation)
HardReset	Writing this bit to '1' **resets** the ASIC, and the bit will be set automatically to zero

8.2.11 Mode Register, Mode (19h)

Table 39. Mode register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Write
Dis_CST_Acc	Reserved	OP_MODE	Dis_Gyro_Z	Dis_Gyro_X	Dis_Acc	Dis_AccT	Dis_CST_GyroZ	Dis_CST_GyroX	Miso_SR	Reserved						Read

Table 40. Mode register bit description. 0 for default operation.

Register bit	Description
Dis_CST_Acc	Disable CST of ACC channel (1 = disable, not useful with EOI function) *
OP_MODE	Operation modes: 1 - Low power mode (Default after reset) 0 - Normal operation mode
Dis_Gyro_Z	Disable Z-Gyro (1 = disable, not useful with EOI function)
Dis_Gyro_X	Disable X-Gyro (1 = disable, not useful with EOI function)
Dis_Acc	Disable accelerometer (1 = disable, not useful with EOI function)
Dis_AccT	Disable accelerometer and temp sensor (1 = disable, not useful with EOI function)
Dis_CST_GyroZ	Disable CST of Z-Gyro **
Dis_CST_GyroX	Disable CST of X-Gyro **
MISO_SR	MISO slew rate control 0 - CMISO 10...85pF, default 1 - CMISO 70...200pF

* In case of disable, offset and sensitivity shift in ACC_Z are visible

** SCC400T series is not validated with CST disabled. Disabling CST affects over-range detection and therefore CST should not be disabled in safety critical applications.

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.12 ACC filter control, A_FILT_DYN (1Ah)

Table 41 ACC filter and dynamic control register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Write
Reserved	ALFILTX	ALFILTY	ALFILTZ	AX_DYN	AX_FILT[2]	AX_FILT[1]	AX_FILT[0]	AY_DYN	AY_FILT[2]	AY_FILT[1]	AY_FILT[0]	AZ_DYN	AZ_FILT[2]	AZ_FILT[1]	AZ_FILT[0]	Read

Table 42 ACC filter and dynamic control register bit description.

Register bit	Description
ALFILTX	ACC LGSX filter selection 0 - 200Hz 3rd order filter 1 - 300Hz 3rd order filter
ALFILTY	ACC LGSY filter selection 0 - 200Hz 3rd order filter 1 - 300Hz 3rd order filter
ALFILTZ	ACC LGSZ filter selection 0 - 200Hz 3rd order filter 1 - 300Hz 3rd order filter
AX_DYN	ACC X output dynamic range selection 0 - nominal dynamic range 1 - nominal dynamic range divided by 4
AX_FILT[2]	ACC X filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter 1xx - 300Hz 3rd order filter
AX_FILT[1]	
AX_FILT[0]	
AY_DYN	ACC Y output dynamic range selection 0 - nominal dynamic range 1 - nominal dynamic range divided by 4
AY_FILT[2]	ACC Y filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter 1xx - 300Hz 3rd order filter
AY_FILT[1]	
AY_FILT[0]	
AZ_DYN	ACC Z output dynamic range selection 0 - nominal dynamic range 1 - nominal dynamic range divided by 4
AZ_FILT[2]	ACC Z filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter 1xx - 300Hz 3rd order filter
AZ_FILT[1]	
AZ_FILT[0]	

Z-axis gyro, ACC and LGS related signals (registers) and status bits are not functional for SCR410T-K03.

8.2.13 Component ID 1 Register, C_ID (1Bh)

Table 43 Component ID 1 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
CID[15]	CID[14]	CID[13]	CID[12]	CID[11]	CID[10]	CID[9]	CID[8]	CID[7]	CID[6]	CID[5]	CID[4]	CID[3]	CID[2]	CID[1]	CID[0]	Read

8.2.14 Traceability 2 Register, T_ID2 (1Ch)

Table 44 Traceability 2 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
Reserved	Reserved	Reserved	Reserved	TID2[3]	TID2[2]	TID2[1]	TID2[0]	ASIC_type[1]	ASIC_type[0]	ASIC_ver[2]	ASIC_ver[1]	ASIC_ver[0]	Reserved	Reserved	Reserved	Read

ASIC_type[1:0]

- 01 – 1DOF ASIC
- 10 – 5DOF ASIC

8.2.15 Traceability 0 Register, T_ID0 (1Dh)

Table 45 Traceability 0 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
TID0[15]	TID0[14]	TID0[13]	TID0[12]	TID0[11]	TID0[10]	TID0[9]	TID0[8]	TID0[7]	TID0[6]	TID0[5]	TID0[4]	TID0[3]	TID0[2]	TID0[1]	TID0[0]	Read

8.2.16 Traceability 1 Register, T_ID1 (1Eh)

Table 46 Traceability 1 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
TID1[15]	TID1[14]	TID1[13]	TID1[12]	TID1[11]	TID1[10]	TID1[9]	TID1[8]	TID1[7]	TID1[6]	TID1[5]	TID1[4]	TID1[3]	TID1[2]	TID1[1]	TID1[0]	Read

9 Application information

9.1 Application Circuitry and External Component Characteristics

See Figure 18 and Table 47 for specification of the external components. The PCB layout example is shown in Figure 19.

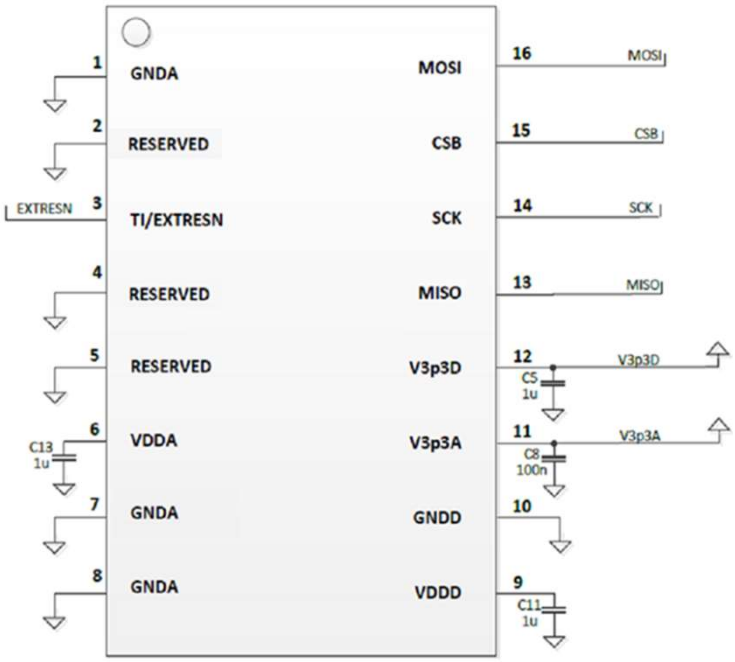


Figure 18. Application schematic.

Table 47. External component description for SCC400T.

Symbol	Description	Min.	Nom.	Max.	Unit
C5	Decoupling capacitor between V3p3D and GND (ESR <100mOhm @ 1 MHz)	0.7	1	1.3	uF
C8	Decoupling capacitor between V3p3A and GND (ESR <100mOhm @ 1 MHz)	70	100	130	nF
C11	Decoupling capacitor between VDDD and GND (ESR <100mOhm @ 1 MHz)	0.7	1	1.3	uF
C13	Decoupling capacitor between VDDA and GND (ESR <100mOhm @ 1 MHz)	0.7	1	1.3	uF

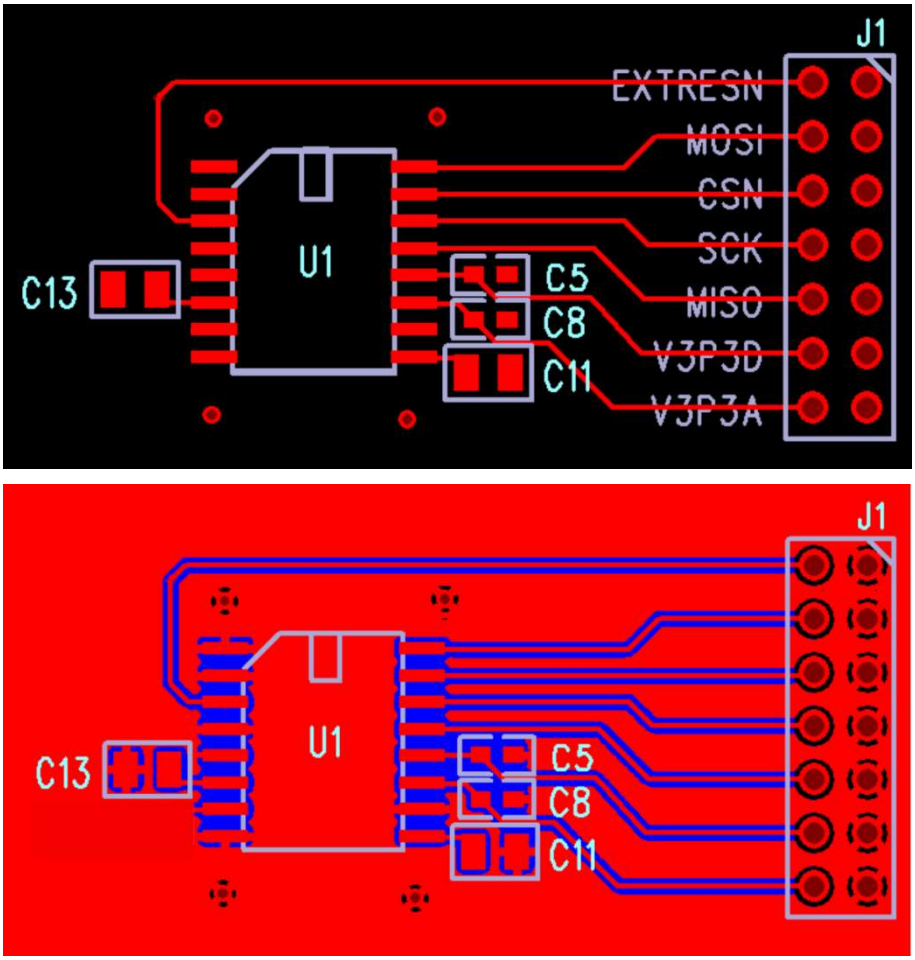


Figure 19. Application PCB layout.

Please see chapter 2.15 for PCB pad dimension recommendation. PCB terminal pads should be wider than package lead to improve solder joint quality. (Recommendation)

Uniform metal plane that is connected to GNDA must be drawn below the component plastic body on the top metal layer (the PCB metal layer on which the component is soldered, see Figure 20). No signal routing is allowed on top metal layer below the component. (Requirement)

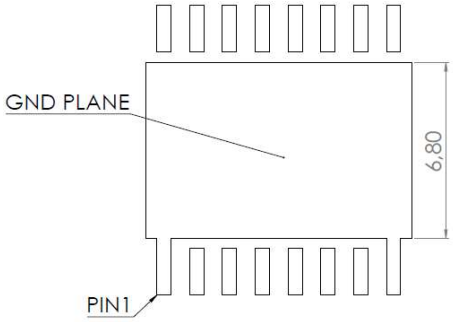


Figure 20. Required top metal layer below component.

Electrically disturbing digital signal lines on top metal layer (the PCB metal layer on which SCC400T component is soldered) have clearance requirement to housing body (Figure 21).

Table 48 lists recommended clearance between signal line on top metal layer and housing plastic body. Restriction does not apply to electrically static signal lines such as VDDD, VDDA,V3p3A, V3p3D, GNDA or GNDD.

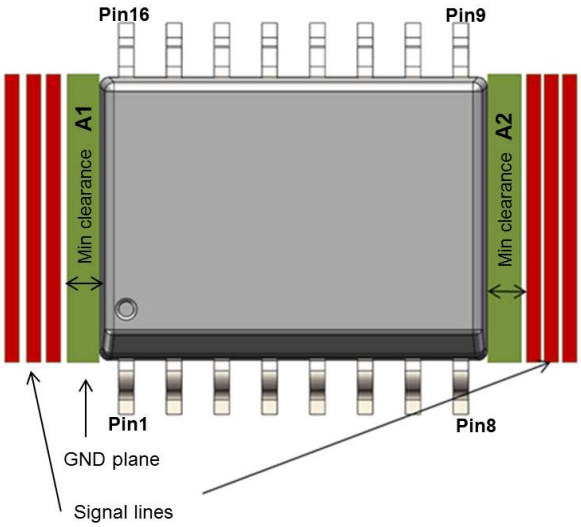


Figure 21. Digital signal lines should have clearance to package housing body.

Table 48. Min. clearance recommendation between signal line and housing plastic body (top metal layer only).

Product type	A1 (mm)	A2 (mm)
SCR410T-K03	1	1
SCC433T-K03	2.5	1

For more details on component application PCB design, design of fixtures, conformal coating, vibration and mechanical shocks, material selections, use application environment, and component assembly process can have an impact on the sensor performance, please refer to the latest version of document “APP 10207 Assembly instructions for SCC400T Series".